FOUR-CHANNEL DIGITAL MIXER/EQUALIZER FOR MASTERING

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1. Abstract

This paper describes the development of a digital audio mixer/equalizer for use in a professional digital audio mastering system with four input channels and two output channels.
This mixer has as good operability as conventional analog audio mixers and has computer-controlled automatic functions. Digital Signal Processors (DSPs) are employed in the system to achieve digital signal equalization and level control which give it good reliability as well as an excellent cost-performance ratio.
The mixer can also be connected to a limiter/compressor and the AES/EBU digital interface. It allows a wide range of applications including the cutting of analog and compact discs, digital audio editing, and the mixing of digital and analog signals such as echo signals.

2. Introduction

The use of PCM technology for the production of music software is growing with the increasing popularity of compact discs (CDs) and VTRs with hi-fi sound (Hi-Fi video). Our commercial PCM mastering system utilizing VTRs developed in response to these trends has already been announced.1), 2)
This system includes a PCM processor, an audio editor, etc. and is widely used not only for the cutting of analog discs but also in mastering for CDs and Hi-Fi video. In this mastering process, sound processing including the modification of tone, the addition of echo and cross-fades from one tune to another is required. But in the past the sound processing of digital signals has to be performed after the signals had been converted to analog; this conversion results in a degradation of sound quality. For these reasons, it became necessary to develop a digital mixer that can process the digital signals as they are without any degradation. This paper outlines the development of a digital audio mixer/equalizer (DMX) for use in mastering with a 4-channel input and 2-channel output which can be used for a wide range of audio processes in CD and Hi-Fi video tape mastering.

3. Design concepts

The DMX was designed to have the functions required in two-channel tape and disc mastering. So that the mastering operation can be performed efficiently, the following design concepts were applied.

(1) Operations should be the same as with a conventional analog mixer, giving the same feeling of operation.

(2) Automated operation should be possible under computer control.

(3) The system should have the flexibility necessary for the connection of a limiter/compressor.

(4) In order to improve reliability and cost-performance, DSPs using LSI technology should be used in the digital signal processing section.

4. Applicability

The DMX is for use mainly as a 2-channel equalizer and as a 4-channel mixer. Fig. 1 shows its use as a 2-channel equalizer.

(1) Copying: With a PCM processor and two VTRs connected to the DMX, it should be possible to perform digital copying while controlling sound quality.

(2) Editing: By adding a digital audio editor to this system, it should be possible to combine editing with copying with sound processing.

(3) CD cutting: The signals reproduced by the PCM processor are processed by the DMX and sent to the CD encoder. By adding a work station to the DMX to increase efficiency, it should be able to perform automatic audio processing. In the automated procedure, first an equalizer pattern is determined and this is saved on a floppy disk in the work station together with the time code. When cutting, by referring to the playback time code, the equalizer pattern is loaded from the disk to the DMX.

Fig. 2 shows an example of using the 4-channel mixer for mastering.

(4) 2-channel digital/2-channel analog mixing: This example shows the mixing of analog and digital signals using a reverberator.
To use various types of reverberators, a D/A converter is provided in the DMX and cue send signals are supplied to the reverberator with the analog signals. The return signal from the reverberator passes through the A/D converter in the processor and is mixed in the DMX.

(5) 4-channel digital mixing: This example shows 4-channel mixing using two PCM processors and two VTRs as signal sources. The last diagram shows an example of the mixed use of AES/EBU format digital signals and the JVC PCM processor.

5. Composition

Fig. 3 is a system block diagram of the DMX; it consists of main and control sections. A control desk, work station and editor are connected to the system control section using RS-422 and RS-232C cables and these control the signal processing section. Details of the signal processing are explained below.

5-1. Equalizer module

Fig. 4 is a block diagram of the equalizer module for one channel. The PCM signal first goes through the 0 to 20 dB attenuator to prevent overflow in the equalizer module. The signal then passes through the emphasis/de-emphasis equalizer with a time constant of 50 µs/15 µs and then to an equalizer which is divided into four ranges.

(1) Equalizer specifications

Fig. 5 shows the characteristic patterns of the equalizer.

Its specifications are:
High range (1.4 kHz - 16 kHz)
Selectable from the following three patterns:
- o Bell type: G: ±15 dB, Q: 0.5 - 3
- o Shelving type: G: ±15 dB
- o Pass type: 12 dB/octave

Mid-high range (600 Hz - 7 kHz)
- o Bell type: G: ±15 dB, Q: 0.5 - 3

Mid-low range (200 Hz - 2.4 kHz)
- o Bell type: G: ±15 dB, Q: 0.5 - 3

Low range (30 Hz - 350 Hz)
Selectable from same three patterns as high range.

(2) Composition of digital filters

Fig. 6 shows the composition of the digital filter used for equalizing in each range. The coefficient is determined by a bi-linear Z transform up to 1.4 kHz. Above 1.4 kHz, because distortion becomes greater using the bi-linear Z transform, a match Z transform is used 3). Problems which appear in hardware design, the coefficient word length and register word length, are resolved as follows 4).

Coefficient word length: In order to minimize the difference from the desired data characteristics and to obtain stability, as is known, the lower the cut-off frequency of a filter, the longer the word length should be. In this filter 27 bits are used in the low and mid-low ranges and 16 bits in the high and mid-high ranges.

Register word length: This determines the signal quality of the filter output. In order to avoid any signal degradation, the register word length must be determined carefully.
When noise increases because of the truncation of the result of an arithmetic operation or the limit cycle, it will cause the signal quality to deteriorate.
Fig. 7 is a graph used to calculate the register word length, that is how many bits are required to maintain 16-bit signal quality in each equalizer stage. The solid line can be calculated from the boundary conditions of noise obtained from the following expression.

$$\text{16-bit quantization noise dispersion} \geqq \text{Noise dispersion after truncation}$$

The dotted line can be calculated from the boundary condition using the following expression.

$$2^{-16} \geqq |\text{Maximum value of limit cycle}|$$

From this graph, it was found that the register word length of the high and mid-high filters used at frequencies over 600 Hz should be 24 bits. For the low and mid-low filters of more than 30 Hz, it was found that a suitable word length would be 35 bits. The hardware word length is set as 39 bits.

(3) Equalizer hardware

In order to design hardware which efficiently satisfies the specifications of the digital filters, DSPs are employed. Although the hardware was conventionally formed using a combination of discrete parts including a multiplier, a memory and TTL components, for the simplification of hardware, DSPs integrated into single LSI chips are used to improve reliability and maintainability; this also makes it possible to reduce costs through mass-production. The DSP devices used in the DMX are μPD77P20s. These chips incorporate 16-bit multipliers and adders and are able to perform extremely high-speed processing; multiplication with accumulation takes only 250 ns.
In addition, the DSP is user-programmable since it incorporates a RAM which can be used for data delay and coefficients and EPROMs for storing coefficients and instructions. As it is provided with serial I/O ports, pipeline processing in which a number of DSP chips are cascade-connected is possible and it is easy to increase the processing capability.

Fig. 8 shows the hardware configuration of a one-channel equalizer. This one-channel equalizer consists of seven DSPs. In the mid-low and low filters, the non-recursive part is processed by the DSP in the earlier stage and the recursive part is processed by the DSP in the later stage given the 39-bit register word length. To maintain the 16-bit accuracy, a 32-bit PCM signal is transmitted serially between each DSP. By loading the respective coefficient from the CPU in the control section to each DSP via the control bus, it is possible to switch the filter characteristics.
Using this method with DSPs, it is possible to install a 4-channel equalizer on a PCB measuring 300 x 280 mm.

5-2. Attenuator/Mixing module

Fig. 9 is a block diagram of the attenuator/mixing (ATT/MIX) module. The 4 channel signals passing through the equalizer module are processed as shown below to output 2 output channels and 2 cue channels. (F and C are attenuation coefficients.)

$$\begin{pmatrix} \mathrm{OUT\ 1} \\ \mathrm{OUT\ 2} \\ \mathrm{CUE\ 1} \\ \mathrm{CUE\ 2} \end{pmatrix} = \begin{pmatrix} F11 & F12 & F13 & F14 \\ F21 & F22 & F23 & F24 \\ C11 & C12 & C13 & C14 \\ C21 & C22 & C23 & C24 \end{pmatrix} \begin{pmatrix} \mathrm{CH\ 1} \\ \mathrm{CH\ 2} \\ \mathrm{CH\ 3} \\ \mathrm{CH\ 4} \end{pmatrix}$$

After calculation, the overflow of the output signal is clipped at a maximum value.
The hardware uses the TMS32010 DSP device. This DSP device makes possible 16-bit parallel input and output and is suitable for processing multiple inputs and outputs as shown in Fig. 9.

5-3. Input/output module

Fig. 10 is a block diagram of the input/output (IN/OUT) module. The DATA I/O module has 6 input channels and 2 PCM output channels; these output channels can be switched to pass through the editor when editing. Time codes used in automatic recording and input/output emphasis flags can also be processed.

The AES/EBU I/O module has 4 input channels and 2 output channels for PCM signals; flag input and output are also possible.

A 2-channel D/A module is provided for the cue send signal, making it possible to provide signals to a conventional analog signal processing unit such as a reverberator.

6. Conclusion

This paper has described a mixer/equalizer for mastering digital audio signals as used in CD, Hi-Fi video systems, etc. The basic design concept is that operations should be similar to those of a conventional analog mixer with automated functions available from a work station; this has resulted in a unit with improved operability. The hardware uses two different DSP devices to improve reliability and cost-performance. The development of this unit will facilitate the production of high quality digital software.

References

(1) Y. Yamada, et al.: "PROFESSIONAL-USE PCM AUDIO PROCESSOR WITH A HIGH-EFFICIENCY ERROR CORRECTION SYSTEM", 66th AES preprint, 1980.

(2) T. Mori, et al.: "ELECTRONIC EDITING IN THE PCM RECORDING USING U-TYPE VTR", 68th AES preprint, 1981.

(3) Masao Kasuga: "DESIGN OF DIGITAL FILTERS FOR VARIABLE ATTENUATION EQUALIZERS", Journal of Acoustical Society of Japan. Vol. 37, No. 1. 1981.

(4) Masao Kasuga, "AN IMPLEMENTATION OF A VARIABLE ATTENUATION EQUALIZER WITH DIGITAL FILTERS". Journal of Acoustical Society of Japan, Vol. 39, No. 4, 1983.

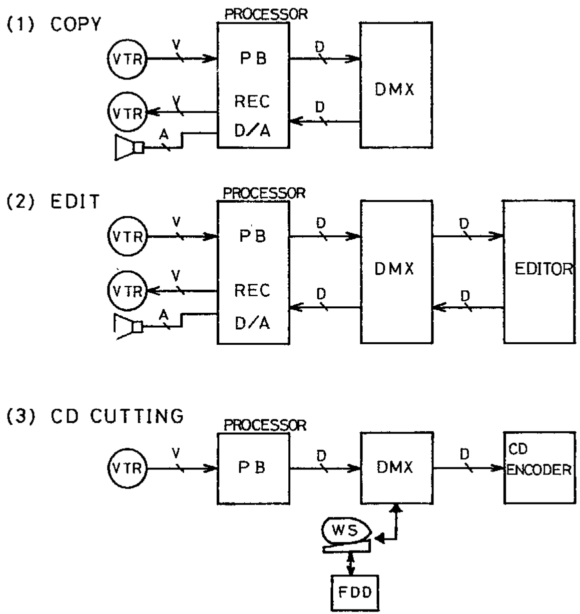

FIG.1 2-CHANNEL EQUALIZER

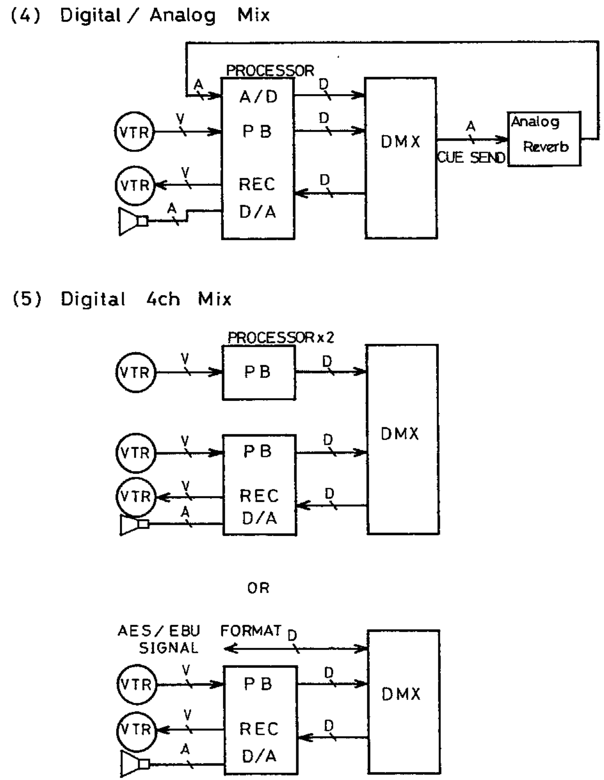

FIG.2 4-CHANNEL MIXER

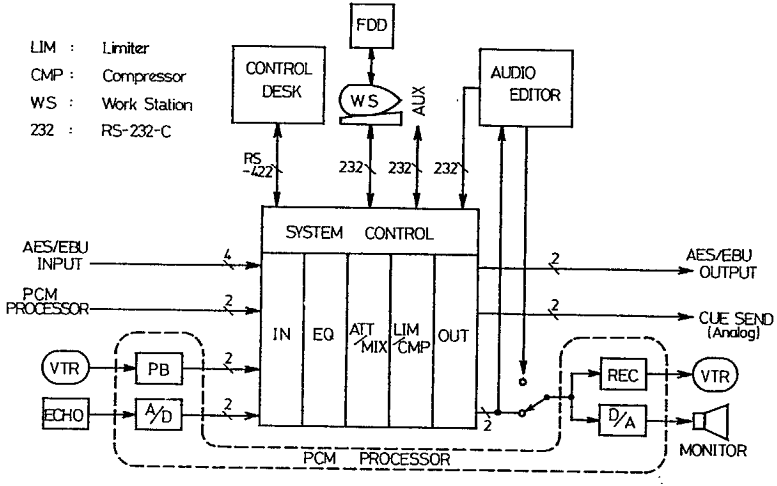

FIG.3 SYSTEM BLOCK DIAGRAM

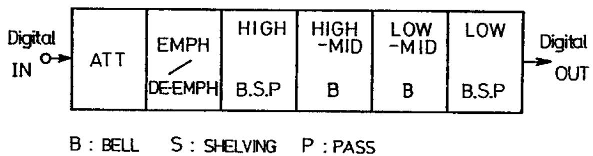

FIG.4 EQUALIZER BLOCK

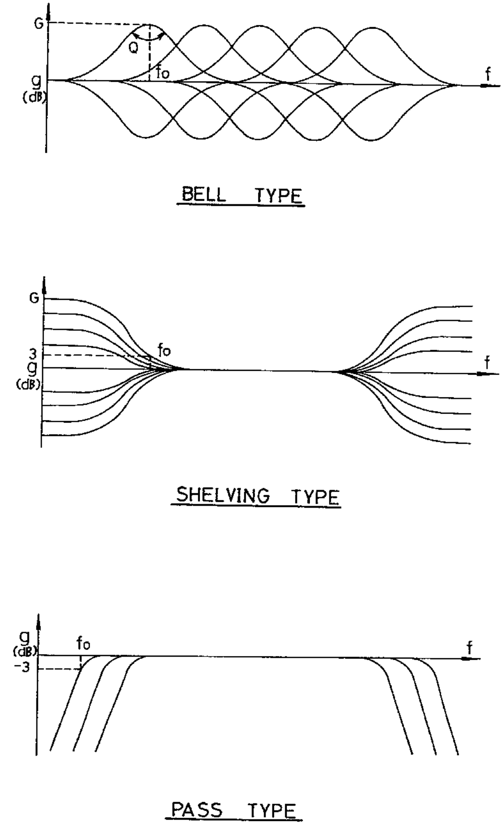

FIG.5 EQUALIZER PATTERN

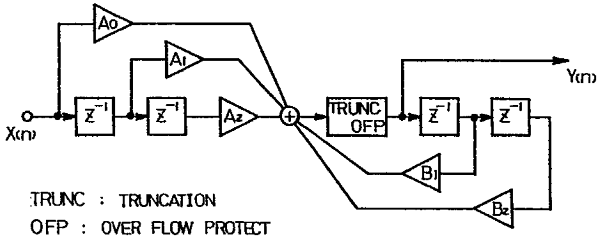

FIG.6 2'ND ODER IIR FILTER

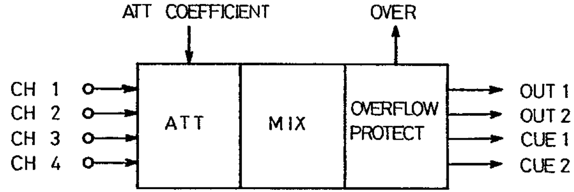

FIG.9 ATT/MIX BLOCK

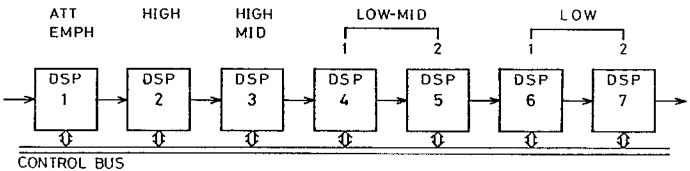

FIG.8 EQUALIZER HARDWARE

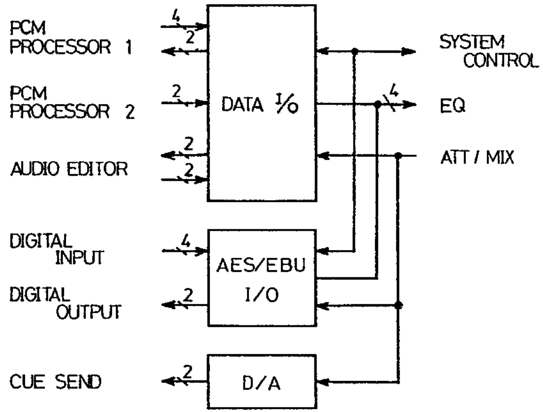

FIG.10 IN/OUT BLOCK

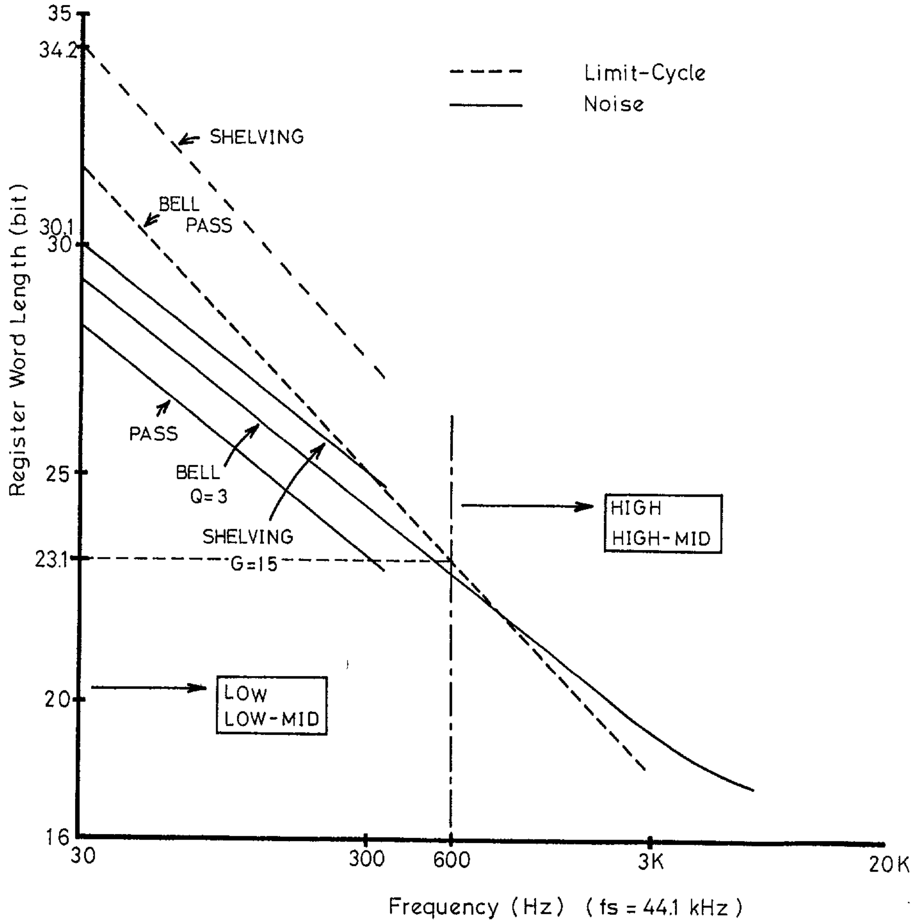

FIG. 7 THE BOUNDARY CONDITION OF REGISTER WORD LENGTH TO AVOID SIGNAL DEGRADATION

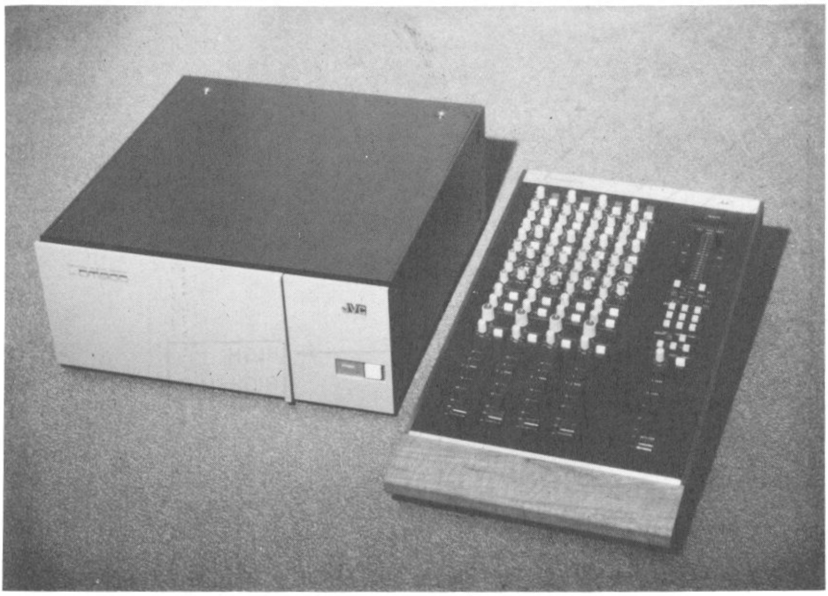

FIG. 8