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Tadashi Abe, Yutaka Hirota, Akira Oinuma,
Takanori Seno, Mitsuo Nabae, Hiromu Niwa,
and Ichiro Yamashita
Matsushita Electric Industrial Co., Ltd.
Osaka, Japan

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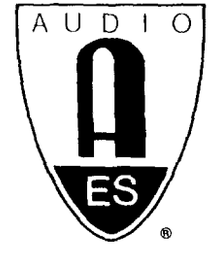

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CUSTOM LSIs, ICS AND DAC FOR COMPACT DISC PLAYER

TADASHI ABE, YUTAKA HIROTA, AKIRA OINUMA, TAKANORI SENO,
MITSUO NABAE, HIROMU NIWA, ICHIRO YAMASHITA

Matsushita Electric Industrial Co., Ltd.
1006 Kadoma, OSAKA 571, Japan

ABSTRACT

The authors have developed 12 custom semiconductor devices for a compact disc digital audio player (4 LSIs, 7 ICs and 1 DAC). The MN6611, 6612 and 6613 LSIs for digital signal processing perform EFM decoding, control and display decoding, and CIRC error correction in the highest grade of error correction and detection. The MN6610 LSI is used for CLV system control.
The AN7670, 7671, 7672, 7673, 7674, 7675 and 7676 ICs are designed for optical head servo control, random trick access and optical deck drive control.
The AN6806 16-bit one-chip DAC has the highest grade of linearity (±0.002%) and a settling time of 0.4μs.

1. INTRODUCTION

Digital audio discs, which are used to play back the PCM-encoded audio signals recorded on their surface, have an exceedingly bright future as one of the supporting pillars of digital audio. The compact disc digital audio system which was developed and putforward in 1980 employs optical digital audio discs using a laser beam for signal readout and it is the system which has won the most enthusiastic support the world over.
The authors are now, however, pleased to report the successful development and practical application of three LSI chips for the digital signal processing section all based on CD standards, an LSI chip for the CLV servo, seven IC chips for optical pick-up control, servo and random access, and a 16-bit DAC chip.

The development of these key devices has paved the way toward achieving higher levels of performance, stability and reliability in compact disc players.

2. FEATURES OF COMPACT DISC PLAYER WITH SEMICONDUCTOR DEVICES

Fig. 1 is a block diagram of the DAD player system which incorporates the newly developed semiconductor devices. All the basic blocks of the system--the optical pick-up servo, the optical pick-up signal processing, the CLV servo, the digital signal demodulator, the random trick play system and DAC sections--have been configured with semiconductors, as the diagram shows.
In particular, meticulous attention was paid to the design of the optical pick-up system ICs in order to do full justice to the performance of the optical pick-up used, and this is an important factor in determining the performance of random trick play.
The flow of the signal processing in the CD player and the basic operations involved will now be described with reference to the block diagram.
The overall system can be broadly divided into 7 functions: the spindle motor control system, the traverse motor control system, the optical pick-up control system, the data slicing and clock regeneration system, the digital signal demodulation system, the system control system and the digital-to-analogue conversion system.

First, the spindle motor system controls the rotational speed so that the linear velocity of the track read out, which is one feature of the compact disc player, is kept uniform. This means that the speed must be high when the data on the inside circumference of the disc are read out and low when the data on the outside circumference are read out. Therefore, in Fig. 1, the present readout position is roughly ascertained by the data of the optical system feed servo, or rather the traverse motor, the speed of the motor is controlled and precise servo is applied so that the readout bit clock is kept uniform.
This is the area comprising the spindle motor, spindle motor drive, CLV control, rough servo control and CLV system control LSI in the Fig. 1 block diagram.
Next, the traverse motor control system functions to extract the desired track of the signals recorded on the disc and it operates in concert with the optical pick-up control system. When the adjustment mechanism of the optical pick-up control system exceeds the uniform deviation, the traverse motor control system is activated so that the track is extracted within the adjustment range at all times.
This is the area comprising the traverse motor, traverse motor drive IC and motor control microcomputor (μCPU) in the Fig. 1 block diagram.

The optical pick-up control system covers the area from the semiconductor laser beam source through the optical sensor to the signal output. It functions to detect the signals in this area, detect the focus error, detect the tracking error, drive and control the actuator and control the disc trick play and random search, among other functions. This area comprises the laser power control IC, head amplifier IC, auto focus IC, matrix operation IC, actuator drive IC and trick play control IC in the Fig. 1 block diagram.

The data slicing and clock regeneration system is composed of the data slicer circuit which slices the output signals from the optical system in the amplitude axis direction and the bit clock regenerator circuit which attains self-synchronization from the output signal of the data slicer circuit. The data slicer circuit features a system which calculates and controls the most appropriate data slice level using a microcomputer based on the error flag data generated from the error correction LSI among the digital signal processing LSIs which will be mentioned later, and its results of this are exhibited to the full in disc compatibility. The clock regeneration system is a dynamic search type of PLL configured with a PLL circuit which is characterized by superlative response, stability and a wide lock range. Its results are exhibited to the full in the response with the generation of burst errors on the disc. This is the area comprising the auto slice μCPU and clock regnerator PLL shown in Fig. 1 block diagram. It has a very significant effect on CD player disc compatibility and on dealing with scratches on the disc and other data dropouts. In other words, it is a key circuit area which requires an approach taking the whole system into consideration.
The digital signal demodulator system provides EFM (eight to fourteen modulation) demodulation for the output signals from the optical system which have been auto sliced and which have passed through the clock regenerator circuit and, after frame synchronization, it provides un-scrambling and de-interleaving processing, and it detects, corrects and interpolates the code errors.
This area also features the approach which takes the whole CD player system into consideration. The fundamental oscillation source of the CD player is the single crystal oscillator in the MN6612 LSI which, with the division of its signal frequency, takes charge of all the player's oscillations, and all the signals are generated from the MN6612 LSI. The reference signal for CLV is also supplied. When it comes to control and display decoding (sub-coding), the P and Q codes are completely decoded while the R - W code is also decoded. Incidentally, a new decoding system of error code detection and correction method is adopted for detecting and correcting the errors in this LSI system, and its effect is extremely remarkable.

This is the area comprising the demodulator LSI, error correction LSI, CIRC control LSI, 4K RAM and 16K RAM in the Fig. 1 block diagram.
The CD player control system is the area which provides centralized control to the operations of the CD player. It deals with the exchanges of data between the MN6611 demodulator LSI and key switch section and all of these operations are performed by the microcomputers. The trick play, search and display functions are controlled. This is the area which comprises the system control µCPU, the 4K RAM and display µCPU in the Fig. 1 block diagram.

Finally, the digital to analogue conversion system covers the area from the MN6612 LSI to the parallel signal output. It provides 16-bit digital-to-analogue conversion and it supplies the signals to the deglitch circuit, filters and 2-channel audio amplifier circuits where the audio signal is produced. This is the area comprising the 16-bit DAC, deglitcher and amplifier in the Fig. 1 block diagram.
The flow of the signals through the CD player has now been described and almost all the functions are carried out by the newly developed semiconductor devices.

3. NEWLY DEVELOPED DECODING METHOD

3.1. CIRC error correcting code

The CIRC error correcting code was developed for detecting and correcting effectively the data errors generated by optical discs. the basic structure of the CIRC error correcting code is shown in Fig. 2.
Four (symbol) parities, P1 - P4, are added to the 28 symbols in one frame represented horizontally in Fig. 2. A further four parities, Q1 - Q4, are added to the 24 symbols shown diagonally. During recording, the focus is first placed on the diagonal direction, arithmetic operation is undertaken for the 24 symbols, W1 - W24, obtained by sampling, and the Q1 - Q4 parities are added. After the time base delay which is called interleaving, the P1 - P4 parities are added for the horizontal direction.
The circuit which arithmetically adds theQ1 - Q4 parities is called the C2 encoder and the circuit which arithmetically adds the P1 - P4 parities is known as the C1 encoder.
Fig. 3 shows the flow of the signal processing in the CIRC encoder.

First, the data equivalent to 1 frame (24 symbols) sent from the AD converter are subjected to a time base operation known as C2 scrambling, and they then enter the C2 encoder. The Q1 - Q4 parities are then arithmetically added in the C2 encoder in accordance with a pre-determined generator polynomial. Interleaving at a distance D = 4 is then im-

plemented for the symbols which enter the C1 encoder. This encoder arithmetically computes the P1 - P4 parities from the 28 symbols and, as a result, one frame has 32 symbol data. Finally, the odd-number symbols are delayed by an amount equivalent to one symbol and, after the data corresponding to parities Q1 - Q4 and P1 - P4 are inverted, they are sent to the EFM modulator circuit.
P1 - P4 and Q1 - Q4 parties, added arithmetically by the CIRC encoder,are defined on a Galois field (2^8) by primitive polynomial.

The Reed Solomon code employed by the C1 and C2 encoders has a parity of 4 symbols in each case and the distance between the codes (d_{min}) is said to be 5.

Generally: $2t_1 + t_2 = d_{min}-1 \cdots (1)$

In this formula, t_1 number of errors can be corrected and $t_1 + t_2$ number of errors can be detected.

Fig. 4 shows the flow of the signal processing with CIRC decoding. This flow is the complete reverse of that characterizing the encoder. Mention is now made of the usual method used in the past for CIRC decoding.

First, the 32 EFM demodulated symbols are C1 unscrambled and they are input into the C1 decoder. This C1 decoder arithmetically computes the 4 syndromes from the 32 symbols, it detects the errors and corrects single errors, and with double or more errors the C1 flag is estbalished. Consequently, there are no errors in frames without the C1 flag (or the errors have been eliminated by single error correction) while double or more errors are present in frames with the flag.

When this kind of operation is undertaken with the C1 decoder, it is possible to detect up to triple errors completely since according to formula (1) $d_{min} = 5$ and $t_1 = 1$. This means that the probability for undetected errors in the C1 decoder is proportional to Ps^4 if the symbol unit error rate is made Ps. This does not mean, however, that all quadruple or more erors remain undetected in the C1 decoder. The Reed Solomon code is defined in GF (2^8) and since only 32 symbols are used in contrast to the maximum code length of 255 symbols, there is an abundance of spaces between the symbols from the viewpoint of distance. As a result, there is a high rate of probability that quadruple or more errors will be detected.
The P1 - P4 parities are removed from the symbols in which single errors have been corrected and double or more errors have been detected by the C1 decoder, and the symbols are de-interleaved along with the C1 flags. It can be

assumed that the C1 flags correspond to the symbols in the ratio of 1:1.
The de-interleaved symbols are now input into the C2 decoder. The Reed Solomon code with a distance between the symbols d_{min} of 5 is also used in this decoder but since the presence or absence of errors is already known by the C1 flags from the C1 decoder, it is possible to correct up to quadruple errors (max. d_{min} -1) . The same error detection operation as with the C1 decoder is performed in the C2 decoder and the errors undetected in the C1 decoder can now be detected.
In this way, up to quadruple errors can be corrected in the C2 decoder but the C2 flag is established in the rare event that uncorrectable errors are produced. This C2 flag is C2 unscrambled along with the symbols which are then aligned in the sequence sampled by the AD converter circuit during recording. Analogue signals are obtained by DA conversion. This concludes the general description of the CIRC code and method used in the past for CIRC decoding.

3.2 New decoding method

The new decoding method which employs the CIRC errror correction system mentioned in Section 3.1 is now described. This new decoding method undertakes double error correction independently for C1 and C2 and it is designed to exhibit its maximum capabilities when it comes to error detection including detection of the miscorrection data. Simulation analysis using a large-scale computer was used in its development.

3.2.1 Decoder operation

The C1 decoder checks the syndromes and sets the error flag during error detection. It also conducts the double error correction operation and when errors cannot be corrected, it sets the C1 flag. The error flag remains set even when correction is undertaken.
The C2 decoder conducts the double error correction operation and when errors cannot be corrected, it sets the C2 flag. Even when detection is possible, it judges between proper correction and mis-correction. With mis-correction, it sets the c2 flag for interpolation.

3.2.2 Mis-correction data detection method and interpolation

The detection method of the mis-correction data, characterized by its greatly enhanced detection capacity, is now described.

If D(E) is defined as the number of places without the error flag which are to be corrected, N(C1) as the number of C1

flags, D(C1) as the number of places without the C1 flag which are to be corrected, N(C2) as the number of errors in C2 and if C(C2) is defined as the number of corrections in C2, then the following cases are judged to be mis-corrections, the C2 flag is set and interpolation performed.

(1) $D(E) \geqq 1$
When at least one symbol without an error flag has been corrected
(2) $N(C1) \geqq 1$ and $D(C1) \geqq 2$
When at least one C1 flag has been set and two or more symbols without the C1 flag are corrected
(3) $N(C1) \geqq 3$ and $D(C1) \geqq 1$
When three or more C1 flags have been set and one or more symbols without a C1 flag are corrected
(4) $N(C1) \geqq 5$ and $C(C2) \geqq 1$
When 5 or more C1 flags have been set and when there is at least one error to be corrected by C2
A transfer is made to interpolation even in the following cases where there is no mis-correction but correction is not possible:
(5) $N(C2) \geqq 3$
When correction is not possible and when there are triple or more errors

In the five cases above, the C2 flag is set and a transfer made to interpolation.
This decoding method, as explained above, is characterized by double error correction independently for the C1 and C2 decoders and by the error flag processing which uses the features of cross interleaving to the full.
For the error correction capability in digital audio optical discs, or rather the compact disc system, the authors developed an error correction algorithm for undertaking extremely sophisticated processing.
Fig. 5 is a block diagram of the new decoding method.

3.3 Error Correction capability of new decoding method

Through the decoding method already mentioned the new error correction system represents a quantum leap in correction capability and in detection capability. The authors used computer simulation for the mis-correction data detection algorithm, and by inputting all the error patterns arising on the discs into the correction circuit, they calculated the error correction leakage and the error detection leakage probabilities.
If, as a result, the correction capability of the new decoding method in a random error state is such that the symbol error rate is made Ps, then the correction leakage probability is expressed as $7.06 \times 10^{10}\ Ps^{9}$, as 7.06×10^{-8} when $Ps = 10^{-2}$ and as 7.06×10^{-17} when $Ps = 10^{-3}$.

The authors conducted simulated computations using a computer to work out the detection leakage probability with each error rate. As a result, this probability was found to be 4.11×10^{-17} when Ps = 10^{-2} and 8.12×10^{-29} when Ps = 10^{-3}.
Similarly, simulated computations using a computer were conducted to work out the interpolation probability. As a result, this was found to be 3.61×10^{-7} when Ps = 10^{-2} and 7.06×10^{-17} when Ps = 10^{-3}.
When the probability of a forcible transfer of a correctable pattern to interpolation was calculated, this was found to be 1.05×10^{-7} when Ps = 10^{-2}.
Accordingly, when the symbol error rate is 10^{-3}, the interpolation probability is once in about 5,000 years and the probability of click noise arising, which is the most serious problem with digital audio error correction systems, or rather the probability of a detection error arising, was similarly found to be of a negligible order when the symbol error rate is 10^{-3}.
Fig. 6 shows the capabilities of the error correction method developed by the authors.

4. LSIS FOR DIGITAL SIGNAL PROCESSING

4.1 Features

The authors focused on the following points when they tackled the development of the LSIs.
(1) Priority to system design
The authors took the approach that the CD player's digital signal processing section was not something that operates independently but something that forms the center of the overall system design. More specifically, this approach consisted in unifying and integrating reliable error correction processing in track jumping caused by disc trick play, protection measures to counter disturbances in the sync. system and the system clock. One result of this is to alleviate the burden placed on the external microcomputers through the incorporation of sub-code demodulation.
(2) Priority to mass production
Consideration was given to the instability at the time of mass producing both the discs and players and as much leeway as possible in the LSI signal processing section was provided. In addition, the LSIs were designed to increase the amount of leeway available in the LSI process.
As a result, the LSIs for the digital signal processing were given a 3-chip configuration. Fig. 7 shows the overall configuration of the LSIs for CD digital signal processing.
Table 1 lists the LSI specifications.
Fig. 8 shows the outlines of these LSIs.

4.2 MN6611 LSI for EFM decoding

Functionally, the MN6611 can be broadly divided into four blocks:

(1) EFM demodulation and generation of signal for CLV servo control
(2) C1 unscramble and jitter absorption
(3) Control data demodulation and transfer to microcomputers
(4) System signal generator circuit for self-checking the LSIs for digital signal processing

The signals are pre-processed in the MN6611 by converting the RF signal read out from the disc into a TTL level digital signal and by regenerating the 4.32MHz clock which coincides with the transmission rate of the signal synchronized with this RF signal using external circuitry.

4.2.1 EFM demodulation

After the EFM signal which has been externally converted to the TTL level has been demodulated to non-return-to-zero (NRZ) using the regeneration clock PCK, it is latched every 14 bits and demodulated into the original 8-bit data. The timing generator and sync. circuit for conducting this demodulation and other signal processing operations are controlled.

4.2.2 C1 unscramble

Compared with tapes, optical discs are subject to more random and relatively short errors. In order to deal with these random short errors in the CD format, C1 and C2 unscramble time base processing is undertaken. With the C1 unscramble, writing is performed by the regeneration clock PCK, reading is performed by the crystal clock MCK and the jitter is also absorbed. Furthermore, the RAM address reset signal is generated.
The RAM address reset signal is generated when the demodulation system has been thrown out of sync, when muting from the microcomputers has arisen and when the integrated value of the time base fluctuations, caused by the jitter or wow/flutter, exceeds the rating.
The jitter margin here is ±4 frames. This represents the value at which 0.42% RMS jitter can be absorbed at the outermost circumference (approx. 200 rpm)
In actual fact, phase control is applied at the frame frequency by the CLV servo and so normally jitter exceeding ±1 frame does not arise.

4.2.3 Address decoder

One of the salient features of the compact disc DAD consists in the recording of control data on the disc and in the use

of these data to allow track search and other operations. The address decoder serves to demodulate these control data and to transfer the results to the microcomputers. The control data are EFM modulated as with the other symbols and recorded on the disc. The address decoder first detects the sync. pattern from among the 14-bit data before EFM demodulation (the control data are completed as a block with 98 frames), generates its own timing and reads out the data. The data consists mainly of the following 3 types:

(1) P data: intervals between tracks and tracks themselves are indicated by "0" and "1."
(2) Q data: track numbers, play time, addresses and other major control data are designated.
(3) R - W data: Standard still undecided; default = "0."

The processing of each type of data is now described.

(1) P data
The P data do not change for 1 block and so the P data in the block are arithmetically processed and transferred to the microcomputers.
(2) Q data
For the Q data 80 bits are effective in 1 block and the remaining 16 bits are redundant bits for error detection. The Q data are written into the internal RAM every 4 bits and they are transferred to the microcomputer at the end of the block. When an error has arisen, all "1"s are sent as the Q data. Busy and Ack signals are employed for handshaking with the microcomputers.
(3) R - W data
Six bits are parallel-to-serial converted per 1 frame and discharged to the microcomputers.

4.2.4 System signal generator

This circuit is designed to test the 3 LSIs (MN6611, MN6612 and MN6613) without using a special checker but by interconnecting them and observing their outputs, and it is provided with a self-check function.

*Functions
(1) EFM signals are output
Three-frame period sine and cosine waves are output to both channels. The address data are output in a 98-frame period.
(2) Dropouts are generated
By activating the mode counter with the CNTL and RESET inputs, six kinds of dropouts can be generated: 1 symbol (1S), 3 symbols (3S), 5 symbols (5S), 5 frames (5F), 9 frames (9F), and 12 frames (12F).

*Features
(1) 3-frame period for EFM data
With the CIRC code 1-symbol delay (1-frame time) is provided with C1 un-scramble, 4n-symbol delay with de-interleave and 2-symbol delay with C2 un-scramble.
Three-frame, 5-frame, 7-frame and other period data can be considered for checking whether the parts are operating (delay) correctly. In this particular case, the 3-frame period was adopted due to the relationship with the ROM capacity and other factors.
(2) 98-frame period for address data
The address data form 1 block with 98 frames. Since the EFM data are repeated in a 3-frame period, the 3-frame period was adopted for the address data too. As a result, a ROM for the address data is provided separately and the data are output at a 98-frame period.
(3) The outputs of (1) and (2) are switched by a counter and the part of the address data in the 3-frame period EFM signals are replaced by the 98-frame period address data.
(4) 8-bit configuration for mode counter
Lower-order 4 bits: Test mode switching
Higher-order 4 bits: Dropout control

4.3 MN6612 LSI for CIRC timing generator and interpolation

The MN6612 LSI is in charge of the area connected to the DA converter from the time base operation in the rear stage of the CD player's digital signal processing section. It can be broadly divided into 4 blocks: system timing generation, de-interleaving, C2 un-scramble and mean value interpolation.
Using the 2.1609MHz clock (MCK), divided down from the 8.6436MHz clock generated by the crystal, as a reference, the system timing circuit generates the basic timing pulses used inside the MN6612 and by the MN6611 and MN6613 and it supplies these pulses as required.
The de-interleaving circuit performs a time base operation to return the interleaved data to their original alignment. The actual data are exchanged between the MN6613 and the external 16K RAM, and the address, read and write signals of the RAM are generated by the MN6612. The flags are processed by the RAM inside the LSI.
The C2 un-scramble circuit performs a time base operation which returns the C2 scrambled data to their original alignment. The data transferred from the MN6613 are un-scrambled by the internal RAM and at the same time converted into timing pulses for D/A conversion. The flags are also simultaneously un-scrambled.
The mean value interpolation circuit performs mean value interpolation or previous data value hold processing for the data which were not corrected in accordance with the flag

information, and it outputs the data. More specifically, the circuit performs preivious data value holding when data have errors continuously of 2 or more words and it performs mean value interpolation when the prior and subsequent data are correct. The DAC output signal is available in offset binary and selection is possible between two modes, 16-bit parallel and serial.

4.4 MN6613 LSI for error correction

The MN6613 LSI for error correction is capable of double error correction and double error detection independently for the C1 decoder and C2 decoder. It is composed of five parts: the syndrome arithmetic, ALU, correction, flag processing and timing generator sections.
The basic operation is such that the syndrome is calculated arithmetically according to the following formula:

$$Si = \sum_{k=1}^{n} (\alpha^i)^{n-k} \quad WK \text{ -------- (2)}$$

Where n = 32 for the C1 decoder
n = 28 for the C2 decoder

Next, the error location polynomial coefficients, 1 and 2, are calculated according to the following formula:

$$\sigma_1 = \frac{S_1S_2 + S_0S_3}{S_1^2 + S_0S_2} \text{ ----- (3)}$$

$$\sigma_2 = \frac{S_2^2 + S_1S_3}{S_1^2 + S_0S_2} \text{ ----- (4)}$$

Similarly, a check is undertaken to ascertain single errors. Next, the error location and error patterns (ei, ej) are arithmetically calculated:

Error location: $\sigma_1 \oplus \alpha j = \sigma_2 \times \alpha^{\gamma}$ $(0 \leqq j \leqq 31)$ --- (5)

Error patterns: $ej = \frac{\alpha^i S_0 + S_1}{\sigma_1}$ ----- (6)

$ei = So + ej$ ----- (7)

Correction is sought from the following formulae:

$$Wi = \hat{Wi} + ei \text{ ----- (8)}$$

$$Wj = \hat{Wj} + ej \text{ ----- (9)}$$

Flag processing is undertaken as described in Section 3.

5. CLV SYSTEM CONTROL LSI

5.1 Features

The MN6610 LSI was developed for CLV system control in the compact disc player and it has the following main functions.

(1) Detection of pick-up position with 2-phase pulse up/down count
(2) Detection of disc end through detection of above position
(3) Programmable divider (for CLV servo) which varies frequency division ratio, based on detection of above position
(4) Data converter (for random access) for converting above position detection data into data on the actual play time base of the disc
(5) Multiplexer and 3-state buffers for supplying above converted data on bus line in byte serial format

The above functions are divided into the following blocks which together configure the actual LSI:
Synchronization, up/down counter, end detector, programmable divider, fixed dividers, data conveter, and multiplexer.
Fig. 9 shows an outline of the MN6611 LSI.
Table 2 lists the basic specifications of the LSI.

5.2 MN6610 LSI

Fig. 10 is a block diagram of this LSI.
The 2-phase pulses from the rotary encoder provided in the feed screw of the pick-up and the drive pulses of the drive motor for moving the pick-up are input into the synchronization block which judges the direction in which the pick-up is moving from the phase relationship of the two input pulses, it selects the up/down counter mode and generates the master clock which controls the operations inside the LSI.
The up/down counter block integrates the pulse signals (SNSA, SNSB) input in synchronization with the pick-up movement and it detects the present position of the pick-up. This is a 10-bit counter with single clock input, up/down mode switching and preset functions.
The disc top and end are detected by a detection gate which prevents overflow and underflow from the range in which the counter is actually used. The END signal is output at a radius greater than that corresponding to the end of the disc's program area.
The programmable divider creates the reference signal required for the CLV servo and its frequency division ratio is set by the higher order 8 bits of the up/down counter.
As soon as the f_{FI} input frequency is constant, the output frequency is made inversely proportional to the contents (= N) of the up/down counter.
The contents of the up/down counter express the pick-up position in terms of a radius but for the display and random access applications it is easier to provide conversion into the actual play time. A ROM is used for this purpose and the data are converted by the data converter.

The multiplexer is provided with functions to divide the 16-bit data output from the ROM into 8 bits each and output these data and it is composed with 32-state buffers to cope with the bus line format. When the data select pin is low, the "minute" data are selected; when the pin is high, the "second" data are selected.
Fig. 11 shows the configuration including the MN6610.

6. ICS FOR OPTICAL HEAD SERVO CONTROL, RANDOM TRICK ACCESS AND OPTICAL DECK DRIVE CONTROL

Table 3 gives the specifications of the ICs which the authors developed for the optical servo, random trick play and traverse drive. The connections of AN7671 and AN7673 from AN7670 which forms the servo loop adopt a current drive system and make for a stable configuration which is immune to fluctuations. AN7671 drives the actuator by current drive using a BTL output system. AN7670 features a low-input-impedance input system which converts the output current of the photo-detector into a voltage.

Fig. 12 shows the outlines of the newly developed ICs.
The basic method behind address search is now described. Address search is performed by reading out the address data recorded on the disc and by moving the optical pick-up by comparing these address data with the desired address. The address data from the MN6611 LSI are compared and arithmetically calculated by a microcomputer and after the traverse stand is moved to the proximity of the desired address, the track is turned "ON" to the desired track finally by the jump signal.
During address search the microcomputer repeats the readout operation of the address data from the MN6611 LSI after the jump signal has been sent to AN7674.

7. 16-BIT ONE-CHIP DAC AN6806

7.1 Features

The AN6806 digital-to-analog converter is the first single-chip monolithic-structured, full-fledged high-speed 16-bit D/A converter to be developed by the industry. It was developed by a high-precision monolithic process technique which combines the bipolar IC process and thin-film resistance process. Its full-fledged performance, such as its high-speed characteristics (settling time: 0.4μs with current output and 3μs with voltage output), high precision (±0.002%/FSR non-linear deviation) and high temperature stability (±0.5ppm/°C of FSR non-linear deviation temperature characteristics), puts the DAC on a par with conventional units used in industrial applications. Furthermore, costs have

been reduced by integrating all the functions on a signle chip while it is possible to make full use of the unit's high speed and process the audio signals of both the left and right channels with a single converter. The AN6806 has a built-in reference voltage source and it does not require any precision external parts. Its precision is ensured by the thin-film resistance laser trimming method and the chip itself is housed in a 28-pin ceramic package.

7.2 AN6806

The approaches aimed at developing low-cost D/A and A/D converters for PCM audio applications are many and varied. The authors chose an approach involving the development of a high-speed and high-precision D/A converter with a combination of current switches based on bipolar ICs, metal thin-film resistor-based ladder resistance networks and the laser trimming technique. The authors decided on this approach for the following reasons.

(1) Current switches based on bipolar ICs are characterized by a high speed and low output capacitance and it is possible to use them to configure high-speed D/A converters which cannot be obtained with CMOS chips. This was an important factor which makes it possible to apply the switches in successive approximation A/D converters
(2) Using bipolar ICs reduces the load on the D/A and A/D converter peripheral circuits and enables converters which are extremely easy to use for users to be created. For instance, it is easy to incorporate a reference voltage source and to ease the restrictions on the output operational amplifier.
(3) Metal thin-film resistors have virtually ideal temperature stability and linearity with respect to voltage for achieving high-precision ladder resistance networks.

Success in the development of the DAC with the above combination was also due to the following techniques.

- High-precision thin-film resistance process and design techniques
- Integration of bipolar IC process and above-mentioned thin-film resistance process
- Design of current switch circuit with high precision and high yield
- Establishment of effective laser trimming technique
- Optimization of circuit layout and creation of high-precision mounting technology

Fig. 13 shows an outline of the AN6806 while Fig. 14 is a block diagram and the basic specifications are given in Table 4.

8. CONCLUSION

The authors have now reported on the newly semiconductor devices and the new decoding method for the compact disc player. Compact disc systems use an optical method to attain noncontact readout and this feature, along with the compact sizes involved, stand the systems in good stead as far as market penetration is concerned.
The authors developed the semiconductor devices for the main signal processing section which is of prime importance in achieving this penetration. The development itself owes a great deal to the advances made recently in the field of semiconductors.

Acknowledgments

The cooperation of a great many technicians and researchers was asked in the development of the semiconductor devices and the authors wish to acknowledge the enthusiastic support as well as the help and advice they received from the personnel of related departments and divisions.
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Because of space restrictions the names of the authors were confined to those of the personnel in charge of the related departments and divisions.

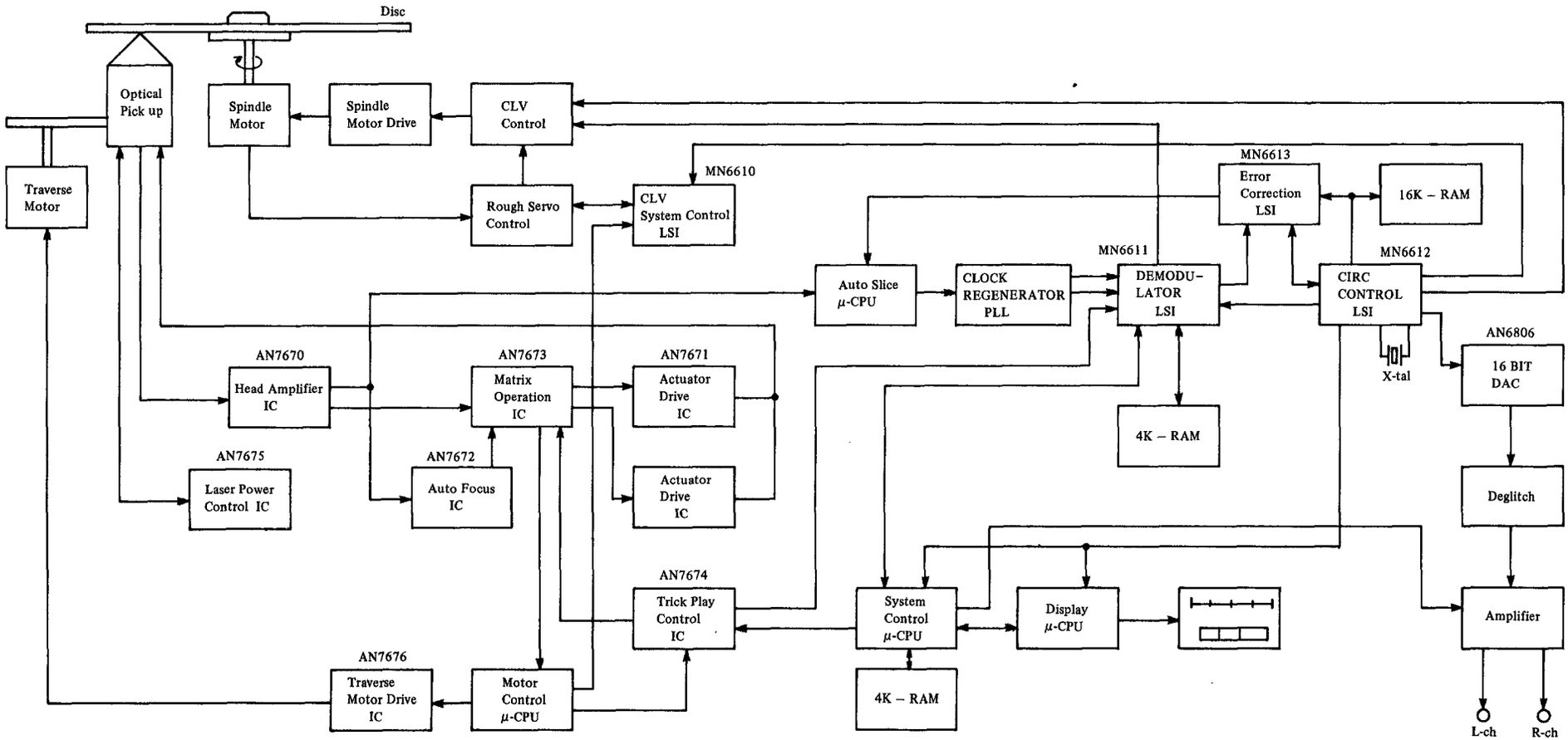

Fig. 1 Compact disc player system block diagram

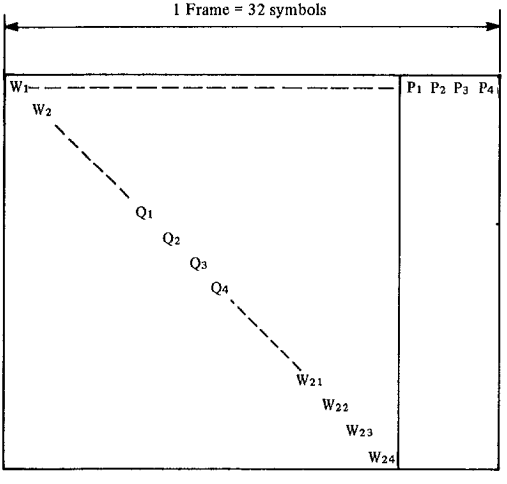

Fig. 2. Basic structure of CIRC

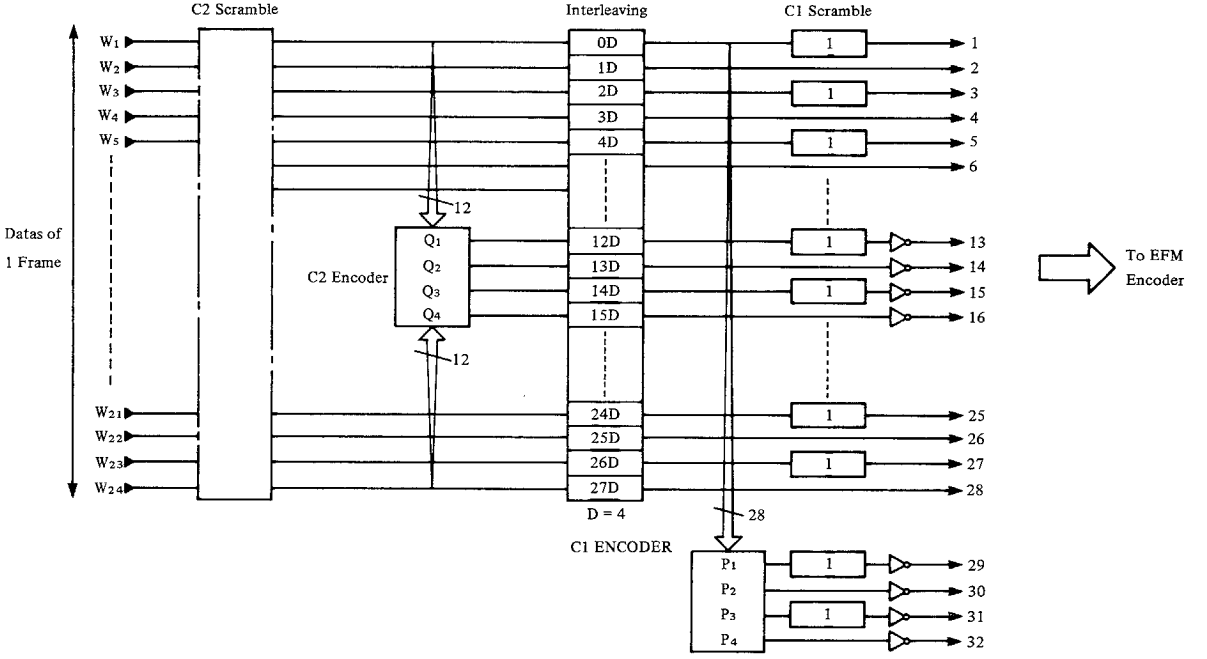

Fig. 3. CIRC Encoder

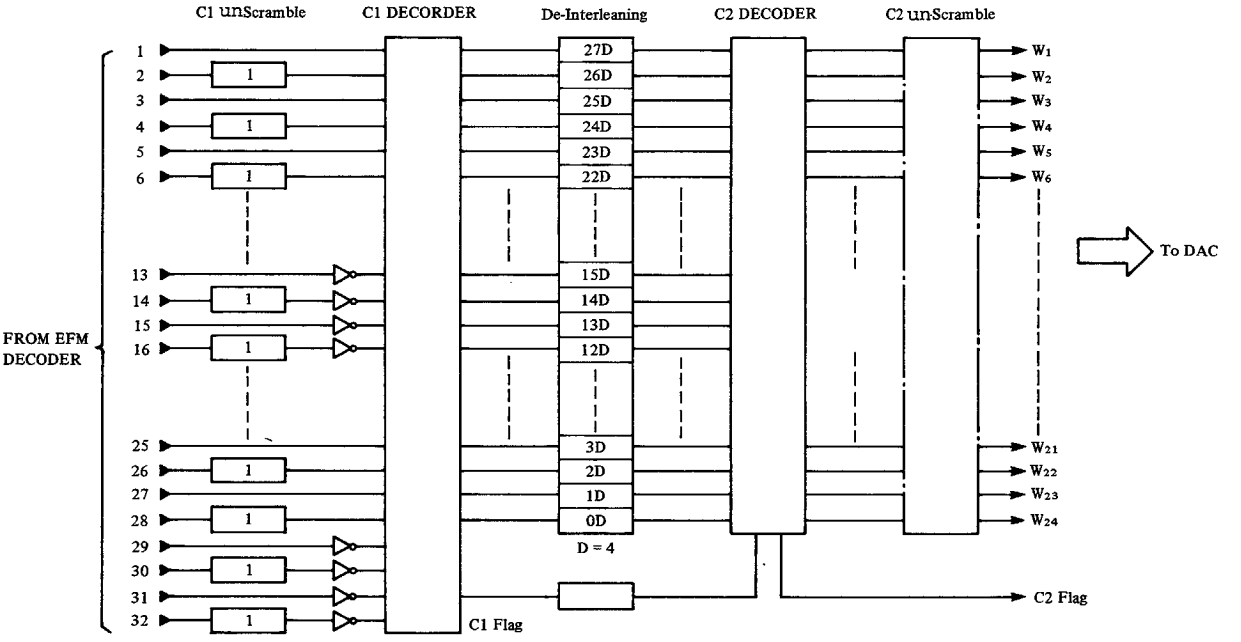

Fig. 4 CIRC Decoder

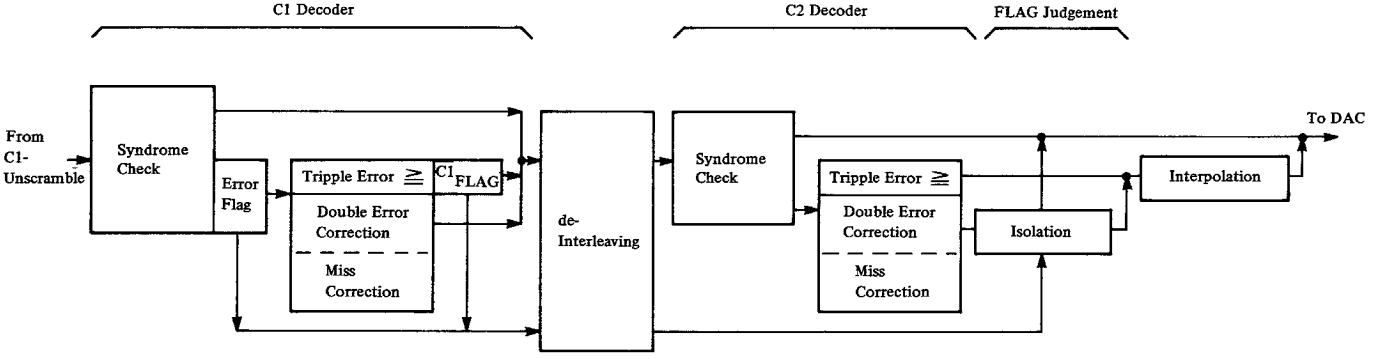

Fig. 5 New Decorder Block Diagram

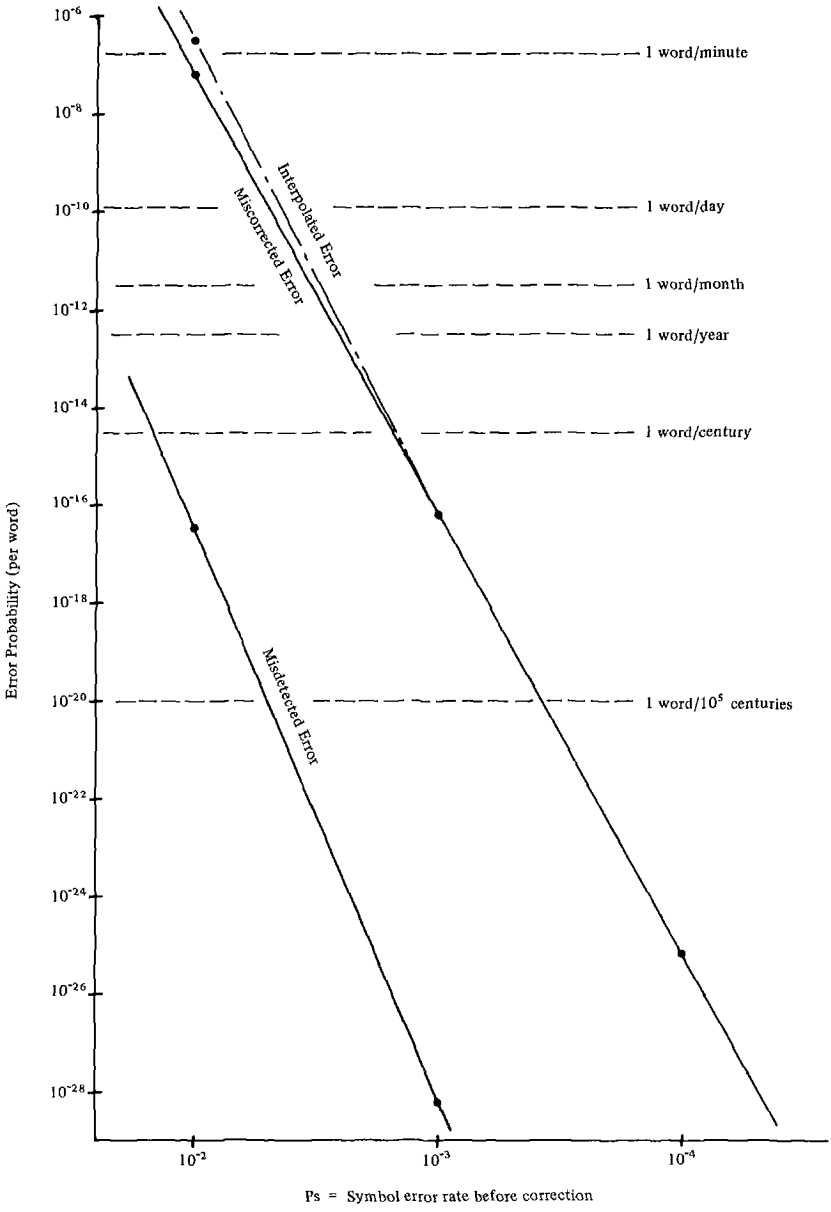

Fig. 6 Performance of New Error Correction System

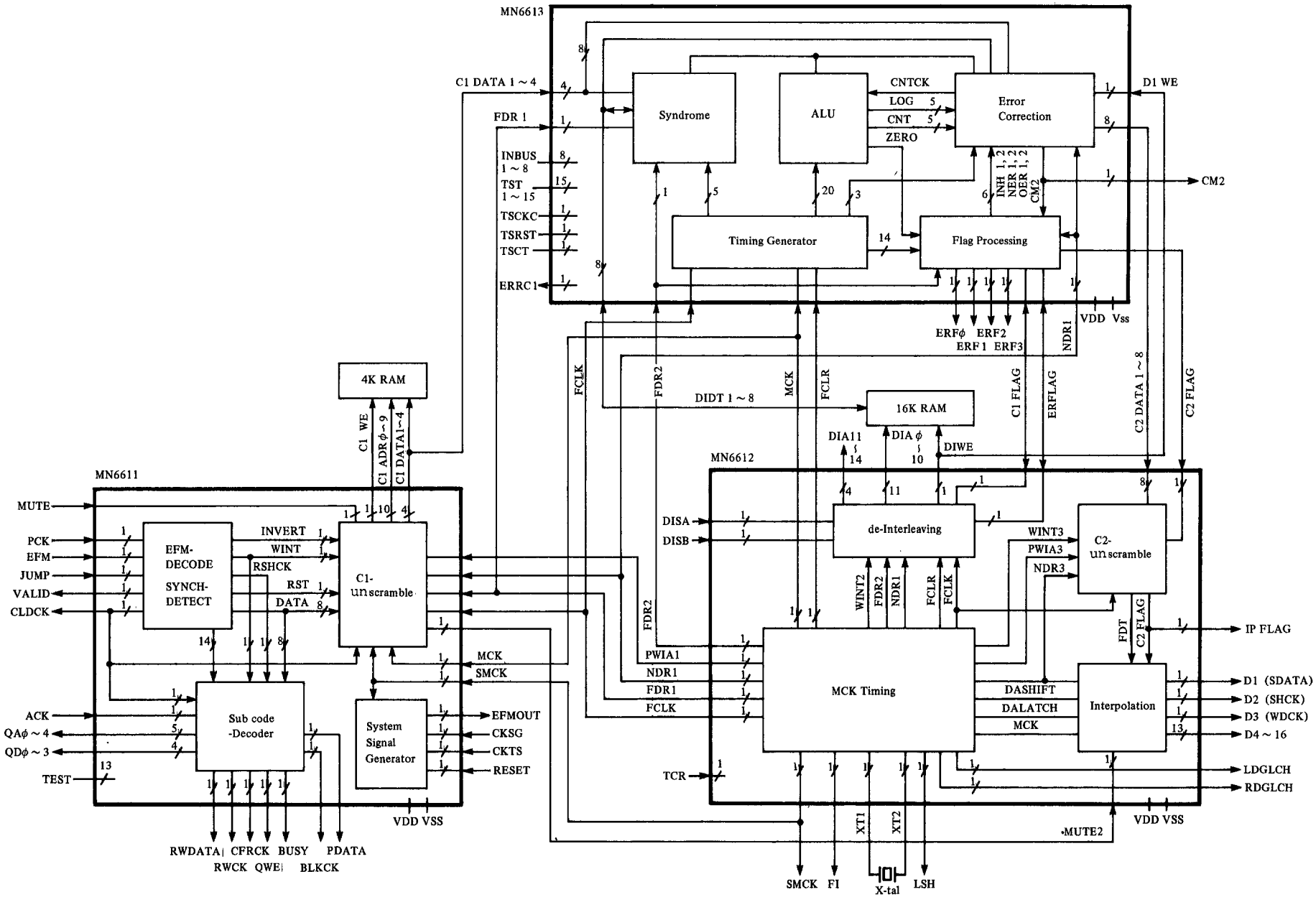

Fig. 7 Digital Signal Processing LSI Block Diagram

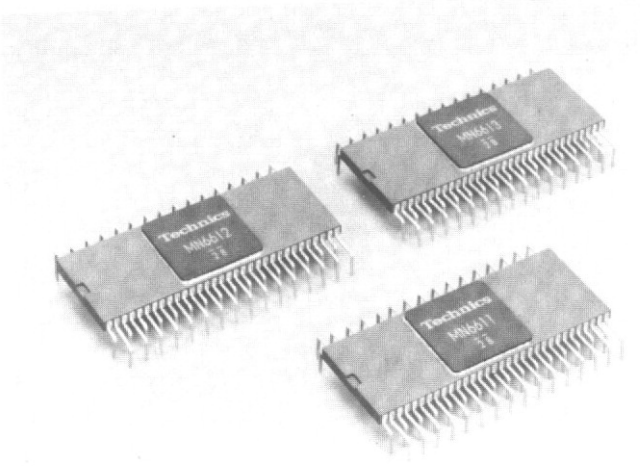

Fig. 8 MN6611 MN6612 MN6613

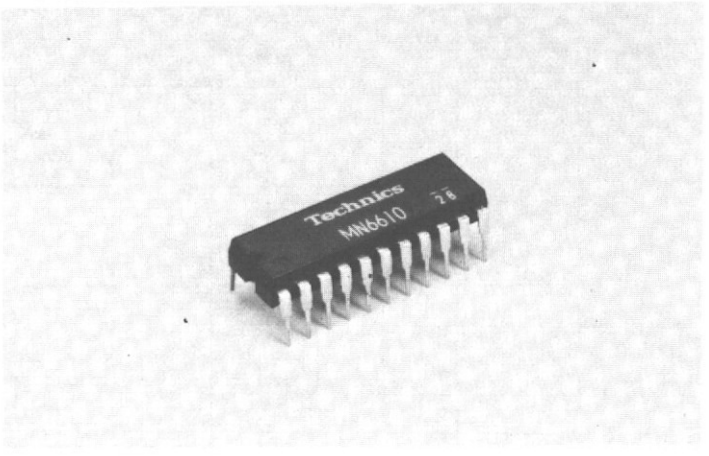

Fig. 9 MN6610

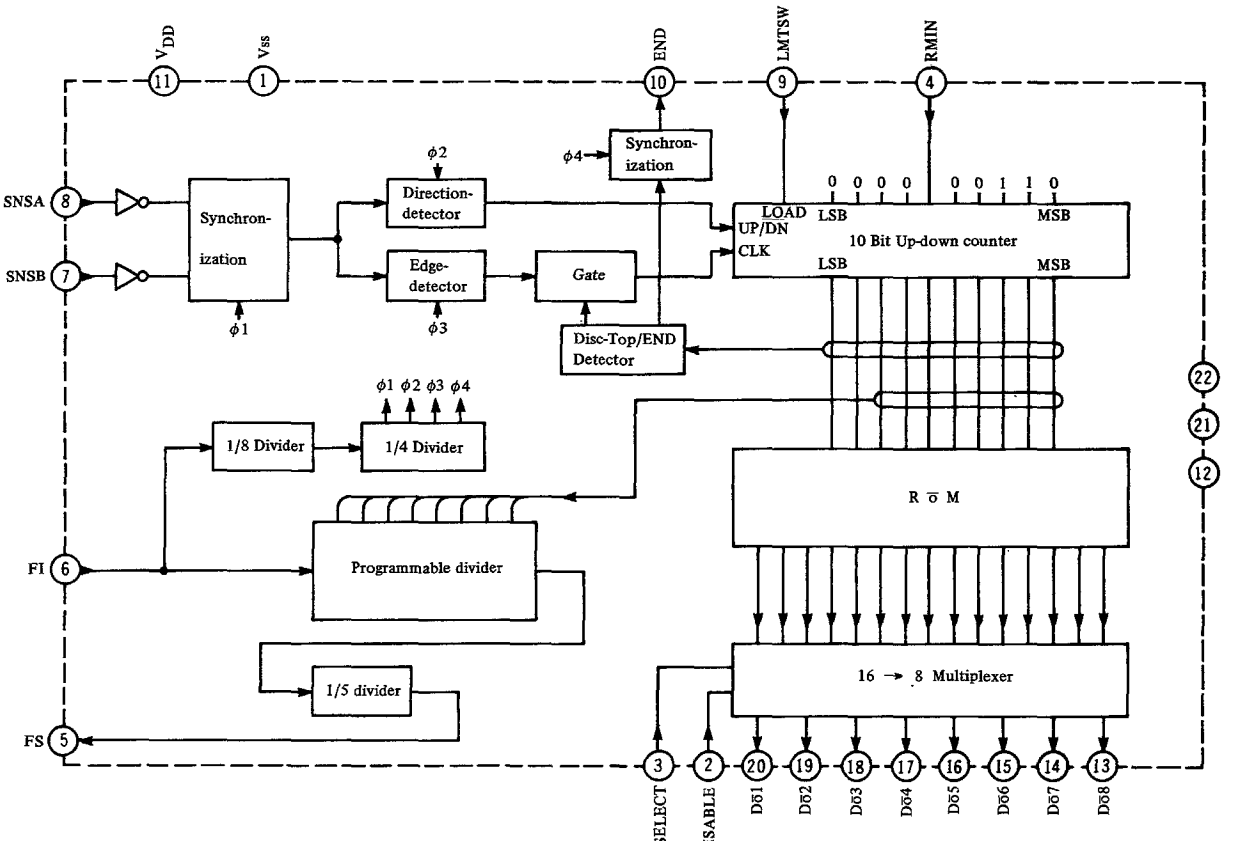

Fig. 10 MN6610 Block Diagram

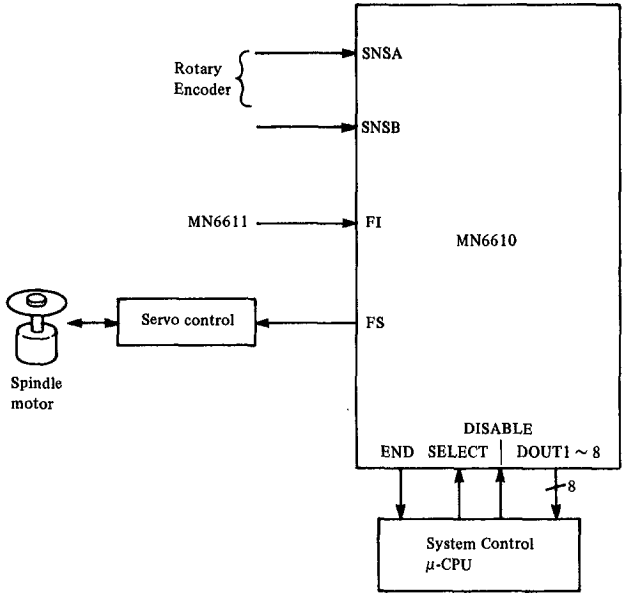

Fig. 11 System Block Diagram for MN6610

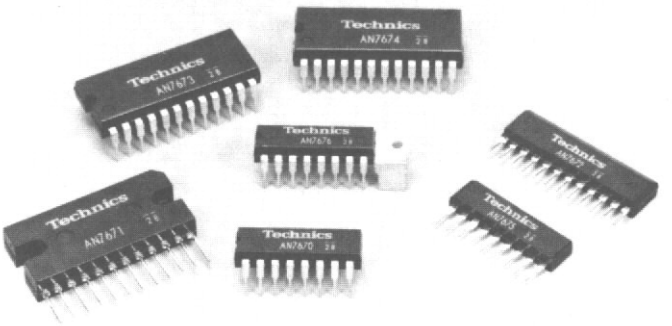

Fig. 12 ICs for Optical head servo control, random trickaccess and Optical deck drive control.

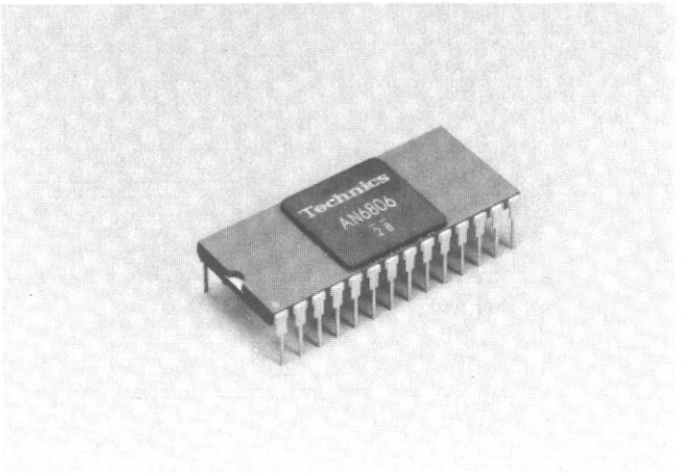

Fig. 13 AN6806

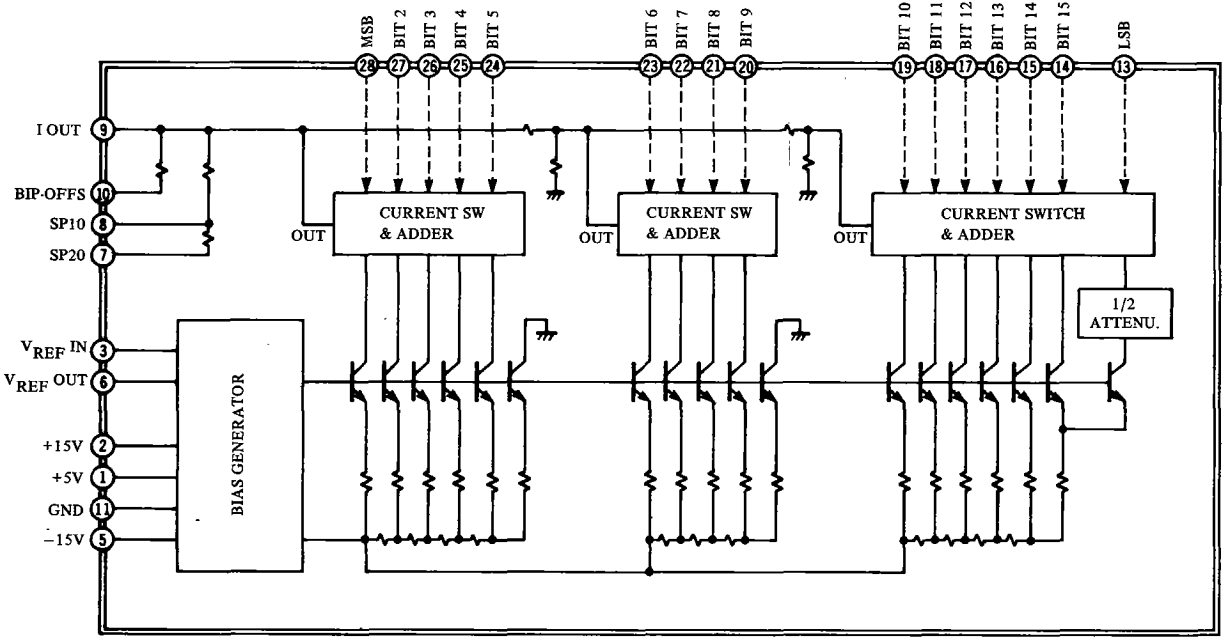

Fig. 14 Functional Diagram of 16 BIT DAC AN6806

Table 1 Basic Specifications of LSI MN6611, MN6612, MN6613

	MN6611	MN6612	MN6613
Process	NMOS 3μ	NMOS 4μ	NMOS 3μ
Chipsize	5.79 mm x 5.33 mm	6.39 mm x 6.57 mm	7.09 mm x 6,78 mm
Transistor	About 13,000 Transistors	About 17,000 Transistors	About 20,000 Transistors
Supply Voltage	+5V	+5V	+5V
Operating Maximum Frequency	6.0 MHz	8.64 MHz	2.16 MHz
I/O Interface	TTL Compatible	TTL Compatible	TTL Compatible
Package	OIL 64 PIN	OIL 64 PIN	OIL 64 PIN

Table 2 Basic Specifications of LSI MN6610

	MN6610
Procese	NMOS 4μ
Chipsize	3.0 mm x 3.9 mm
Transistor	About 10,000 Transistors
Supply Voltage	+5V
Operating Maximum Frequency	305 kHz
I/O Interface	TTL Compatible
Package	DIL 22 PIN

Table 3. Basic Specifications of ICs

	AN7670	AN7671	AN7672	AN7673	AN7674	AN7675	AN7676
Naming	Head Amp	Actuator Drive	Auto Focus	Signal Processing	Trickplay	Laser APC	Traverse Motor
Process		High Voltage Power				High Voltage	High Voltage Power
Chipsize	2.10mm x 1.60mm	2.50mm x 2.40mm	1.90mm x 1.70mm	2.45mm x 2.00mm	2.70mm x 2.20mm	1.35mm x 1.30mm	3.00mm x 2.00mm
Transistor	122 Transistor	106 Transistor	115 Transistor	200 Transistor	318 Transistor	58 Transistor	47 Transistor
Supply Voltage	+12V	+15V	+12V	+12V	+12V, +5V	−15V	+15V
Package	DIL 16 PIN	SLI 12 PIN Power	SLI 12 PIN	DIL 24 PIN	DIL 24 PIN	SIL 9 PIN	DIL 16 PIN FIN

Table 4. Basic Specifications of AN6806

	AN6806
Resolution	16 BITS
Linearity	± 0.002%/FSR
	± 0.5 PPM/°C FSR
Settling Time	0.4 μsec.
Digital I/O	TTL compatible
Supply Voltage	+15V, +5V, −15V
Package	DIL 28 PIN