

Signal Processing of the Compact-Cassette Digital Recorder

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The signal-processing techniques for compact-cassette digital recording are of interest to those concerned with consumer audio equipment. A cassette digital tape recorder using a metal-evaporated tape has been developed together with a high-density ferrite head having 12 tracks of 120- μm track width and 0.3- μm gap length per channel. Specially designed digital signal-processing circuits include circuits for signal generation, modulation, error correction, and signal control. The digital modulation scheme called FEM-4 is a new and key item of the design. The practical design and system concepts are outlined.

0 INTRODUCTION

When the Compact Disc system was introduced to the Japanese market, audio enthusiasts showed keen interest in the system, and Compact Disc players began disappearing from the market because of hardware shortages. Demand has now developed for a consumer digital audio tape recorder (DAT), a system that permits digital recording as well as playback.

DAT system developments were announced by several companies, followed by demonstrations at audio shows. The systems developed are not compatible with each other, since tape and signal formats are different. We see a high potential for DAT systems in the consumer market, and as hardware manufacturers we feel a responsibility to disclose our own system concepts as a step toward future standardization.

Recording media and conversion electronics are also important, and are described in a companion paper. In this paper we deal only with the DAT system concept, the digital modulation scheme, and the error-correction scheme.

1 RECORDING DENSITY

Recording density in digital tape recorders, both stationary-head and rotary-head types, increases gradually following development in recording tape, magnetic heads, recording equalization, tape speed control, error correction, digital modulation, and the tape-transport mechanism.

Fig. 1 plots the relationship between linear density

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and track density for various systems and shows clearly that these quantities should be higher for a DAT than for the conventional analog system. These are the causes for most of the difficulties. Moreover, the relationship between these factors is complex. For instance, the required linear density depends on the digital modulation scheme, track density, sampling rate, quantization, tape speed, and so on. Suitable recording density depends also on an adequate playing time and on the reliability desired in a tape recorder for consumer use.

2 STATIONARY HEAD VERSUS ROTARY HEAD

Consumer requirements include small size, low price, light weight, high quality, and easy operation. Fig. 1 compares stationary-head with rotary-head recording.

Compared with rotary-head systems, a stationary-head system has higher recording density but lower track density. The area density of both systems is generally considered to be 10 M bit/in²-20 Mbit/in². The packing bit density, however, will soon be increased if a new recording technology such as perpendicular recording is introduced.

For many consumers a cassette system is the best way to handle and store recordings. The cassette arrangement is also effective in protecting digital recordings from dust, fingerprints, and breakage. Editing capability is another factor essential for ordinary music recording. Accordingly, fast cuing operation as well as quick response in stop, start, and standby modes are important. Since an intricate mechanical structure increases cost, a compact-cassette digital system has advantages over a rotary-head (VCR) recorder. These were our reasons for choosing a stationary-head system.

3 TAPE FORMAT

For two-channel operation with a 44.1-kHz sampling frequency and 16-bit quantization the required bandwidth for digital audio signals is 1.5–2 MHz, and recording and reproduction are not possible with conventional heads and tape speed. Multiple tracking is usually applied to keep the recording frequency per track sufficiently low. The number of tracks and the tape speed must be chosen according to the characteristics and the performance of the head and the recording characteristics of the tape.

Both bulk type or thin-film type heads are available. The former are suitable for short-wavelength recording, the latter for multitrack recordings.

For digital recording we have developed an advanced evaporated tape and have chosen a ferrite head in combination with this tape.

An increased number of tracks makes the track width narrower, degrades the signal-to-noise ratio, and makes the head susceptible to dropout from dust and tape flaws. A highly accurate tape-transporting mechanism and uniform tape width are also required, which conflicts with the simplicity of a compact-cassette recorder. Crosstalk increases as well. Accordingly, a trial 12-track head was made to minimize the number of tracks. Fig. 2 shows the tape format. The track width is 120 μm , and the track spacing is 35 μm .

The two-channel audio signals are distributed to 10 tracks, and two auxiliary tracks are provided. One purpose of the two auxiliaries is to record parity in order to permit error correction when any two out of the 10 data tracks are subjected to long-term code error from dropouts. A second purpose is for random-access ad-

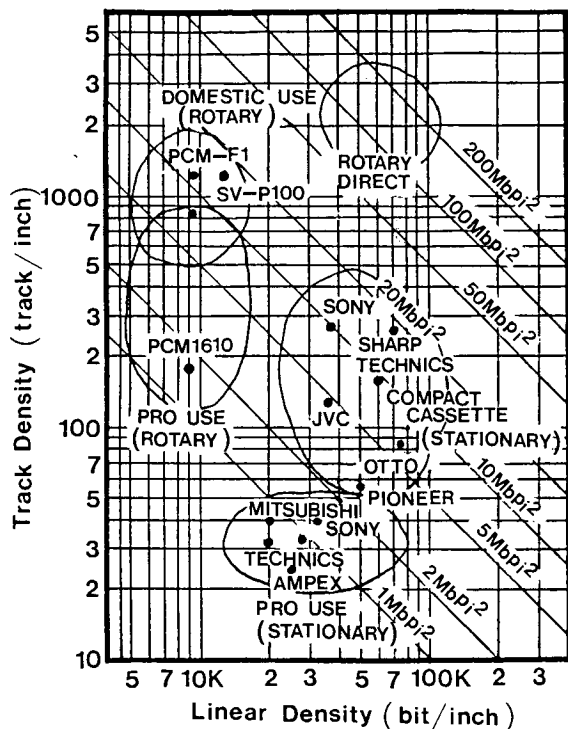


Fig. 1. Recording density.

dress and other control signals (such as capstan servo).

The multitrack head is a combination type for recording and reproduction. The gap length is set at 0.3 μm for the presumed recording wavelength of 1–1.5 μm . Fig. 3 shows an external view of the experimental head.

4 SIGNAL FORMAT

Fig. 4 shows examples of the signal format. The sample in Fig. 4(a) is for a compact cassette using 44.1-kHz sampling frequency, 16-bit quantization, and two channels to realize a performance equivalent to that of the Compact Disc. The sample in Fig. 4(b) is for a microcassette, which has a nonlinear quantization system with 32-kHz sampling frequency.

The signal format comprises the synchronous data of 8 bits and user data of 8 bits. One frame for compact cassette consists of 8 data words, error-correcting code

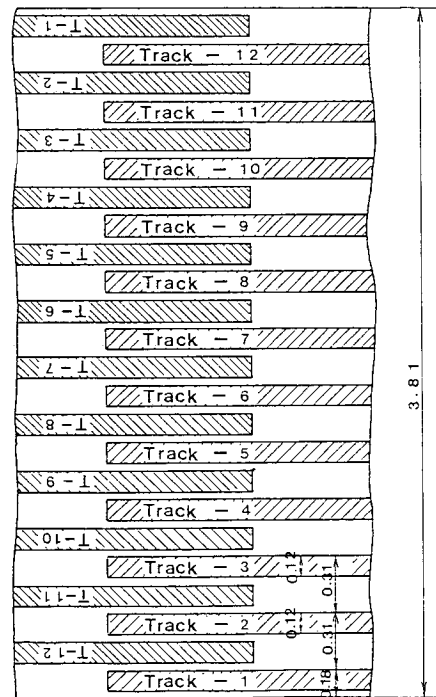


Fig. 2. Tape format.

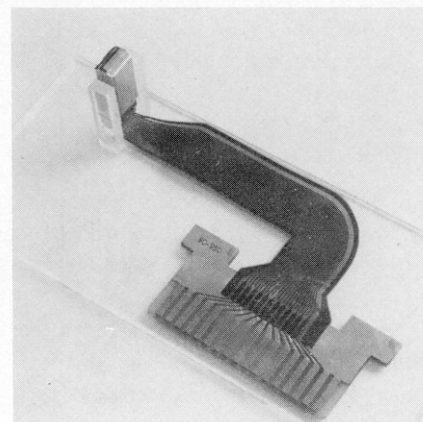


Fig. 3. Multitrack ferrite head.

P and Q, and error-detecting code CRCC (cyclic redundancy check code).

The data word and the error-correcting code P and Q are subjected to an adequate interleave treatment. In the tape-track direction the addition of parity R is possible for every five tracks, and the configuration is effectively resistant to single-track trouble.

5 DIGITAL MODULATION SYSTEM [1]-[3]

The recording rate in one track is 211.68 kbit/s, and recording is not possible with conventional modulation because of the recording wavelength. With Modified Frequency Modulation (MFM) the recording wavelength is 0.89 μm if the tape speed is 95 mm/s and the code error will increase. With 3 Position Modulation the wavelength is 1.34 μm and recording and reproduction are possible. For the compact cassette, however, jitter will increase, and a modulation system with shorter maximum length between transitions is required. We have therefore developed a modulation system exclusively for the compact cassette and the microcassette so as to realize high-density recording and reproduction.

The conditions generally required for the modulation system are

- 1) Wide window margin T_w
- 2) Small maximum length between transitions
- 3) Large minimum length between transitions
- 4) Large density ratio
- 5) Small error propagation at demodulation
- 6) Easy self-locking
- 7) Small number of handling bits (m, n) for a conversion.

The well-known MFM and 3PM have been used for digital recorders, and both are run-length limited code.

3PM has the same T_w as MFM, but T_{min} and Density Ratio (DR) are 1.5 times as large, and T_{max} is 3 times as large ($6T$).

The new system is a four-to-eight modulation type in which the binary data of 4 bits are converted to coded words of 8 bits. T_{min} and DR are the same as for 3PM, and the length between transitions is 1.5-4.5T. The window margin is 0.5T.

The system is called FEM-4. The maximum length between transitions T_{max} is improved by as much as 25% from 6T of 3PM to 4.5T. The hardware can be realized rather easily with some gate arrays. Table 1 shows the conversion table of FEM-4, and Fig. 5 is an example of the hardware structure. In the drawings,

- En: = original data
- En + 1: = Data word before original data in time series
- En - 1: = Data word after original data in time series
- Pn, X: = Xth bit of modulation data to original data En
- Pn + 1, X: = Xth bit of modulation data to original data En + 1.

The original data are expressed in the hexadecimal system as shown above. To the combinations shown under

the right-hand column of Table 1 a special modulation rule is applied.

A new digital modulation system, FEM-5, was also developed in which T_{max} is improved by 33.3%, from 6T of 3PM to 4T. The algorithm and the hardware configuration of this system are a little more intricate. Table 2 shows the conversion table and the algorithm. Because of hardware limitations, FEM-4 is now used. Table 3 compares the new and the conventional systems.

Fig. 6 illustrates the generation probability versus the length between transitions (related to clock regeneration and bit synchronization capability) for the new

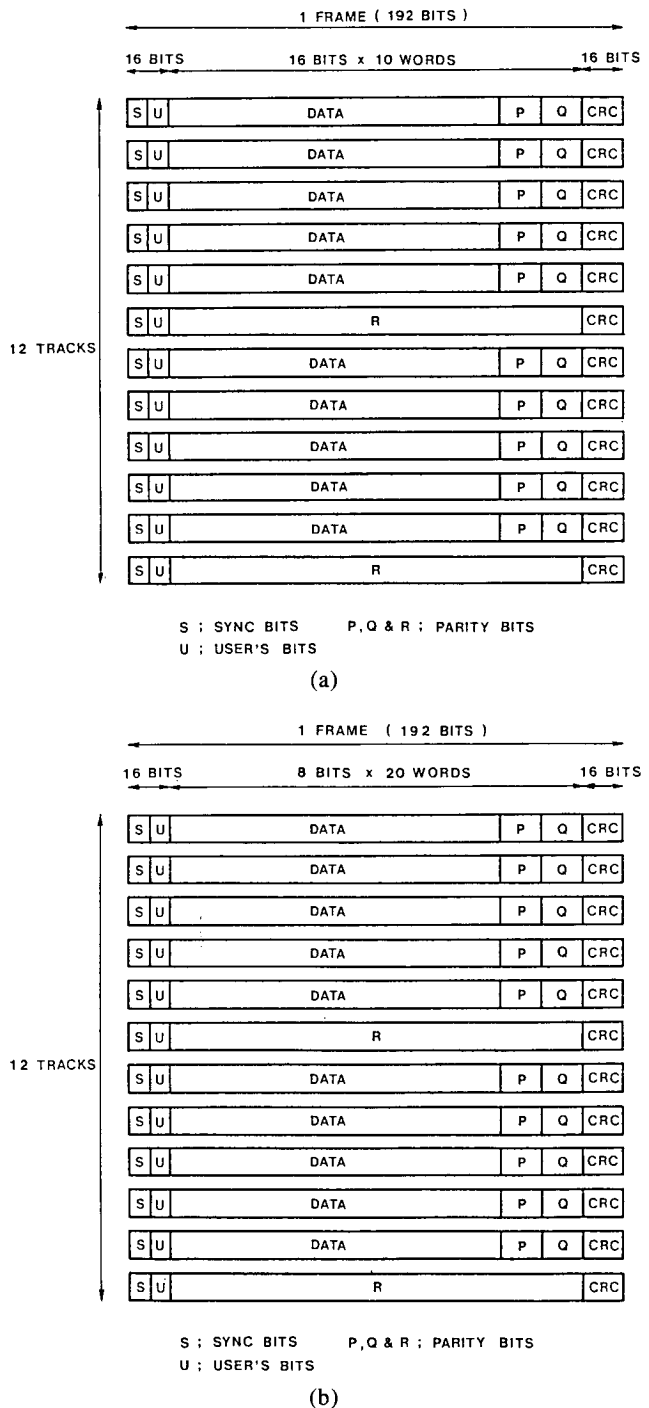


Fig. 4. Example of signal format. (a) Compact cassette. (b) Microcassette.

modulation systems and for FEM-1, whose performance is equivalent to that of conventional 3PM.

With high generating probability of short lengths between transitions, the bit synchronization and clock pull-in capability are greater. As the comparison shows, the phase tolerance of the system to jitter is larger because T_{max} is shorter than that of 3PM. Advantages of the higher transition probability are the followup to jitter under normal conditions and quick pull-in synchronizing after a long-term signal suspension due to such troubles as dropout.

Table 1. Data conversion in FEM-4.

no.	ORIGINAL E_n	MODULATION DATA(1)	MODULATION DATA(2)
		$P_{n,i}$ i/12345678	$P_{n,i}$ i/12345678
1	0000	00000010	00001000
2	0001	00000100	
3	0010	00010000	
4	0011	00100000	
5	0100	01000000	01001001
6	0101	00010010	
7	0110	10010010	
8	0111	00100100	
9	1000	01001000	
10	1001	10010000	
11	1010	10000010	
12	1011	00100010	
13	1100	01000010	
14	1101	01000100	
15	1110	10000100	
16	1111	10001000	

Table 2. Data conversion in FEM-5.

no.	ORIGINAL E_n	MODULATION DATA(1)	MODULATION DATA(2)	MODULATION DATA(3)
		$P_{n,i}$ i/12345678	$P_{n,i}$ i/12345678	$P_{n,i}$ i/12345678
1	0000	00000010	00001000	00001001
2	0001	00000100		
3	0010	00010000		
4	0011	00100000	10001001	
5	0100	01000000	01001001	
6	0101	00010010		
7	0110	10010010		
8	0111	00100100		
9	1000	01001000		
10	1001	10010000		
11	1010	10000010		
12	1011	00100010		
13	1100	01000010		
14	1101	01000100		
15	1110	10000100		
16	1111	10001000		

MODULATION RULE IN FEM-5

*1. IF $E_{n+1} E_n = (20)_{16}$ THEN $P_{n+1,8} = 1$
 $= (30)$ $P_{n,3} = 1$
 $= (40)$
 $= (90)$
 $= (F0)$
 $= (21)$
 $= (31)$
 $= (41)$
 $= (91)$
 $= (F1)$

6 DIGITAL SIGNAL PROCESSING

To the data sampled at 44.1 kHz and quantized to 16 bits by an analog-to-digital converter, the error-correction code P and Q, a synchronizing signal, and the error-detection code CRCC are added, and then distributed to each track, modulated, and transferred to the recording circuit of each track.

The reproduced signals are subjected to waveform equalization and then transmitted to clock-regeneration and synchronizing-extract circuits in pulse form. Sub-

MODULATION RULE IN FEM-4

*1. IF $E_{n+1} E_n = (20)_{16}$ THEN $P_{n+1,8} = 1$
 $= (30)$ $P_{n,3} = 1$
 $= (40)$
 $= (80)$
 $= (90)$
 $= (F0)$
 $= (21)$
 $= (31)$
 $= (41)$
 $= (91)$

*2. IF $E_{n+1} E_n = (42)_{16}$
 $= (45)$
 THEN $P_{n+1,1} \sim P_{n+1,8} = 01001001$

*3. IF $E_{n+1} E_n = (10)_{16}$ AND $E_{n-1} = (6)_{16}$
 $= (70)$ $= (9)$
 $= (D0)$ $= (A)$
 $= (E0)$ $= (E)$
 $= (F)$

THEN $E_n = 00001000$

*4. IF $P_{n+1,7} P_{n+1,8} P_{n,1} = 101$
 THEN $= 010$

*2. IF $E_{n+1} E_n = (42)_{16}$ AND $E_{n-1} = (2)_{16}$
 $= (43)$
 $= (45)$
 $= (47)$
 $= (4B)$
 $= (80)$
 $= (81)$

THEN $P_{n+1,1} \sim P_{n+1,8} = 01001001$

*3. IF $E_{n+1} E_n = (10)_{16}$ AND $E_{n-1} \gg (0)_{16}$
 $= (70)$
 $= (D0)$
 $= (E0)$

OR $= (00)$ AND $E_{n-1} = (6)$
 $= (50)$ $= (9)$
 $= (60)$ $= (A)$
 $= (A0)$ $= (E)$
 $= (B0)$ $= (F)$
 $= (C0)$

THEN $P_{n,1} \sim P_{n,8} = 00001000$

*4. IF $E_{n+1} E_n = (10)_{16}$ AND $E_{n-1} = (0)_{16}$
 $= (70)$ $= (1)$
 $= (D0)$
 $= (E0)$

THEN $P_{n,1} \sim P_{n,8} = 00001001$

*5. IF $E_{n+1} E_n = (32)_{16}$
 $= (35)$
 THEN $P_{n+1,1} \sim P_{n+1,8} = 10001001$

*6. IF $P_{n+1,7} P_{n+1,8} P_{n,1} = 101$
 THEN $= 010$

Table 3. Comparison of parameters in various modulation systems.

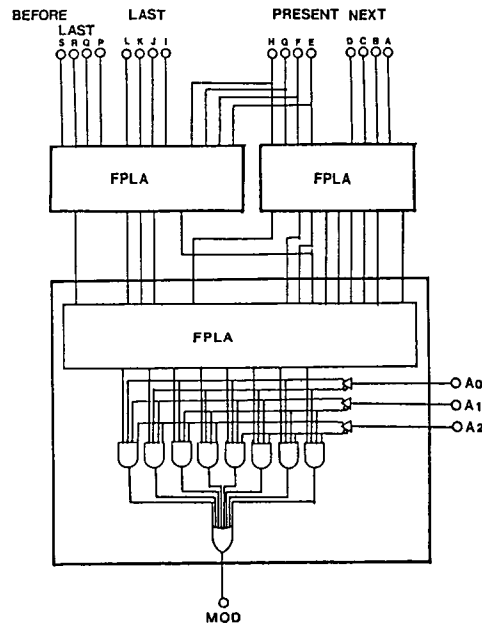
Method	T_w	T_{min}	T_{max}	Bit Sync		DR	$T_{min} \times T_{max}$
NRZ/NRZI	T	T	00	X	X	1	1
PE/FM	$T/2$	$T/2$	T	O	O	1/2	0.25
MFM	$T/2$	T	$2T$	O	X	1	0.5
M	$T/2$	T	$3T$	O	X	1	0.5
4/5MNRZI	$4T/5$	$4T/5$	$12T/5$	O	X	4/5	0.64
3PM	$T/2$	$1.5T$	$6T$	O	X	1.5	0.75
HDM-1	$T/2$	$1.5T$	$4.5T$	O	X	1.5	0.75
HDM-2	$T/2$	$1.5T$	$4T$	O	X	1.5	0.75
HDM-3	$T/3$	$2T$	$25T/3$	O	X	2	0.67
FEM	$0.47T$	$1.41T$	$5.18T$	O	X	1.41	0.66
IDM	$T/2$	T	$2T$	O	X	1	0.5
FEM-4	$T/2$	$1.5T$	$4.5T$	O	X	1.5	0.75
FEM-5	$T/2$	$1.5T$	$4T$	O	X	1.5	0.75

sequently the signals are demodulated and tested for error detection.

Demodulated data of each track have absorbed jitter, and the error correction in the track-width direction is executed if parity is added in the track-width direction.

After rearrangement for unification, error detection and correction are made again, and the data are then converted into analog signals by a digital-to-analog converter. Fig. 7 shows the outline of this signal processing.

Differing from conventional hardware design, a microprogramming method is introduced into the digital signal processing. The signal processor has a composition similar to that of a commercial digital signal processor and includes 1) microprogram memory, 2)



$$MOD = A0 * A1 * A2 * P1 + A0 \sim * A1 * A2 * P2 + A0 \sim \sim * A1 \sim * A2 * P3 + A0 \sim \sim * A1 \sim \sim * A2 * P4 + A0 * A1 * A2 \sim * P5 + A0 \sim * A1 * A2 * P6 + A0 * A1 \sim * A2 \sim * P7 + A \sim * A1 \sim \sim * A2 \sim \sim * P8$$

WHERE

$$P1' = E \sim * F * G + E \sim * F * H + F * G * H + E * F \sim * G \sim * H$$

$$P2' = E \sim * F \sim * G + E \sim * F \sim * H + F \sim * G * H$$

$$P3' = E * F * G \sim + E * F * H \sim$$

$$P4' = E \sim * F * H \sim + E * F \sim * G * H \sim + E * F \sim * G \sim * H$$

$$P5' = E \sim * F \sim * G \sim * H + E * F * G * H$$

$$P6' = E * F \sim * G \sim * H \sim + E * F * G * H \sim + E \sim * F * G * H$$

$$P7' = E \sim * F \sim * G \sim * H \sim + E * F \sim * G * H \sim + E \sim * F * G * H \sim + E \sim * F \sim * G * H + F * G \sim * H$$

$$P8' = 0$$

$$P8'' = B \sim * C \sim * D \sim * F * G \sim * H * + A \sim * B \sim * C \sim * D \sim * F \sim * G \sim * H + B \sim * C \sim * D \sim * E \sim * F \sim * G * H \sim + B \sim * C \sim * D \sim * E * F \sim * G \sim * H + A \sim * B \sim * C \sim * D \sim * E * F * G * H$$

$$P3''' = P3' + F \sim * G \sim * H \sim * J * K \sim * L \sim + E \sim * F \sim * G \sim * H \sim * J \sim * K \sim * L + F \sim * G \sim * H \sim * I \sim * J \sim * K * L + F \sim * G \sim * H \sim * I * J \sim * K * L + E \sim * F \sim * G \sim * H \sim * I * J * K * L +$$

$$P8'''' = P1' + A \sim * B * C \sim * D \sim * E \sim * F * G * H \sim + A * B \sim * C * D \sim * E \sim * F \sim * G * H \sim$$

$$P5'''' = P5' + A \sim * B * C \sim * D \sim * E \sim * F \sim * G * H \sim + A * B \sim * C * D \sim * E \sim * F \sim * G * H \sim$$

$$W0 = E \sim * F \sim * G \sim * H \sim$$

$$X = R6 * W0 * N1$$

$$P5'''' = P5'''' + X$$

$$P7'''' = P7'''' * X$$

$$P1'''' = P1'''' (R7'''' + R8'''')$$

$$P7'''' = P7'''' (P8'''' + N1 \sim)$$

$$P8'''' = P8'''' + P7'''' * N1$$

$$P1 = P1''''$$

$$P2 = P2''''$$

$$P3 = P3''''$$

$$P4 = P4''''$$

$$P5 = P5''''$$

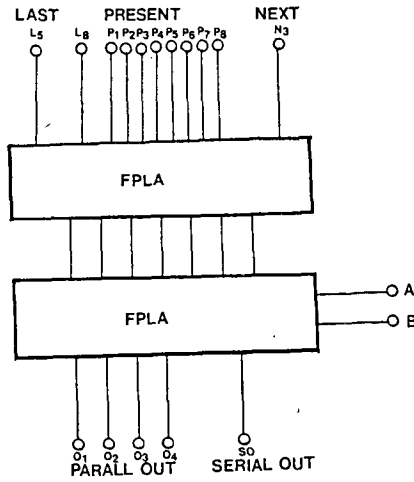
$$P6 = P6''''$$

$$P7 = P7''''$$

$$P8 = P8''''$$

~ indicates inverse

Fig. 5(a). Example of modulation circuit for FEM-4.



$$\begin{aligned}
 O1 &= S1^{\sim} * S3^{\sim} * S4^{\sim} * S5^{\sim} * S6 * S7^{\sim} + S1^{\sim} * S2^{\sim} * S3 * S4^{\sim} * S5^{\sim} * S7^{\sim} \\
 &+ S1^{\sim} * S2^{\sim} * S3^{\sim} * S4 * S5^{\sim} * S6^{\sim} * S7 + S1 * S2^{\sim} * S3^{\sim} * S4 * S5^{\sim} * S6^{\sim} * S7^{\sim} \\
 &+ S1^{\sim} * S2^{\sim} * S3 * S4^{\sim} * S5^{\sim} * S6^{\sim} + S1 * S2^{\sim} * S3^{\sim} * S4^{\sim} * S5 * S6^{\sim} * S7^{\sim} \\
 O2 &= S1^{\sim} * S2^{\sim} * S3^{\sim} * S4^{\sim} * S5^{\sim} * S6^{\sim} * S7^{\sim} + S1^{\sim} * S2^{\sim} * S3 * S4^{\sim} * S5^{\sim} * S7^{\sim} \\
 &+ S1 * S2^{\sim} * S3^{\sim} * S5^{\sim} * S6^{\sim} * S7 + S1^{\sim} * S2^{\sim} * S3 * S4^{\sim} * S5^{\sim} * S6^{\sim} \\
 &+ S1 * S2^{\sim} * S3^{\sim} * S4^{\sim} * S5^{\sim} * S6 * S7^{\sim} + S1 * S2^{\sim} * S3^{\sim} * S4^{\sim} * S5 * S6^{\sim} * S7^{\sim} \\
 O3 &= S1^{\sim} * S2 * S3^{\sim} * S4^{\sim} * S5^{\sim} * S6^{\sim} + S2^{\sim} * S3^{\sim} * S4 * S5^{\sim} * S6^{\sim} * S7 \\
 &+ S1^{\sim} * S2^{\sim} * S3 * S4^{\sim} * S5^{\sim} * S6 * S7^{\sim} + S1^{\sim} * S2 * S3^{\sim} * S4^{\sim} * S5^{\sim} * S7^{\sim} \\
 &+ S1 * S2^{\sim} * S3^{\sim} * S4^{\sim} * S5^{\sim} * S6 : S7^{\sim} + S1 * S2^{\sim} * S3^{\sim} * S4^{\sim} * S5 * S6^{\sim} * S7^{\sim} \\
 O4 &= S1^{\sim} * S2 * S3^{\sim} * S4^{\sim} * S5 * S6^{\sim} * S7^{\sim} + S1 * S2^{\sim} * S3^{\sim} * S4 * S5^{\sim} * S6^{\sim} * S7^{\sim} \\
 &+ S1 * S2^{\sim} * S3^{\sim} * S4^{\sim} * S5^{\sim} * S6^{\sim} * S7 + S1^{\sim} * S2^{\sim} * S3 * S4^{\sim} * S5^{\sim} * S6^{\sim} * S7 \\
 &+ S1^{\sim} * S2 * S3^{\sim} * S4^{\sim} * S5^{\sim} * S6^{\sim} * S7 + S1^{\sim} * S2 * S3^{\sim} * S4^{\sim} * S5^{\sim} * S6 * S7^{\sim} \\
 &+ S1 * S2^{\sim} * S3^{\sim} * S4^{\sim} * S5^{\sim} * S6 * S7^{\sim} + S1 * S2^{\sim} * S3^{\sim} * S4^{\sim} * S5 * S6^{\sim} * S7^{\sim} \\
 K8 &= L8 * P3^{\sim} & V &= J8 * P1 * P2 * Q5 \\
 S3 &= P3 * L8^{\sim} & S5 &= Q5 * V^{\sim} \\
 Q8 &= P8 * N3^{\sim} & Q7 &= P7 + V \\
 J8 &= L5^{\sim} * K8 & S1 &= J8 + P1 \\
 Q5 &= P5 * Q8^{\sim} & S7 &= Q7 + R8 \\
 R8 &= P5^{\sim} * Q8 \\
 S0 &= A * B * O1 + A * B^{\sim} * O2 + A^{\sim} * B * O3 + A^{\sim} * B^{\sim} * O4
 \end{aligned}$$

(b)

Fig. 5(b). Example of demodulation circuit for FEM-4.

microprogram sequencer, 3) arithmetic and logic unit, 4) error counter, 5) data memory, 6) interleave memory, 7) matrix arithmetic circuit, 8) input and output, 9) modulation and demodulation circuit, and 10) synchronizing extraction and clock-regeneration circuits. The system can be changed simply by rewriting the memory and without changing the hardware. Fig. 8 shows the outline of this processing.

7 HOW TO DETERMINE CODE ERROR—THE ERROR-CORRECTING SYSTEM

Causes of code error in digital recording are

- 1) Intrinsic defects of the recording medium, such as defective magnetic material
- 2) Defects on the medium made during operation, such as finger prints, flaws, or dust deposited during use
- 3) Faults of the reproducing mechanism, such as track derailing or disordered capstan servo
- 4) Variation of reproduced signal level
- 5) Jitter
- 6) Noise

7) Intersymbol interference.

These can cause random error or burst error. To correct code errors so caused, interleaving to scatter the data in the longitudinal (track) direction of the tape is ordinarily combined with an error-correction code and error detection. The interleave length (distance) is determined by either of the following two methods.

1) Gilbert model [4]. The interleave time *m* is the

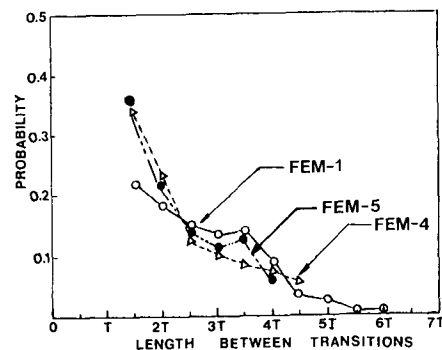


Fig. 6. Generation probability of length between transitions.

time in which the generation probability $\Pr(B)$ of having an error in the n th bit after a burst generation settles to a certain value Z_2 (or t_2).

2) Dropout run distribution. The maximum dropout length of the dropout distribution is taken as the interleave distance.

The greater distance of 1) or 2) is taken as the interleave length.

The Gilbert model was proposed as a simple statistical analysis method of code errors which occur continuously in transmission circuits, and is defined by the transition probability between no-error condition G and error condition B , as shown in Fig. 9.

If the parameters of the Gilbert model are $S_{11} = p$, $S_{12} = P$, $S_{21} = Q$, and $S_{22} = q$, it can be shown by

the following linear transition probability matrix:

$$S = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} = \begin{bmatrix} p & P \\ Q & q \end{bmatrix} \quad (1)$$

Since the number of signals reproduced is quite large, the bit stream given by the Gilbert model may be taken as a constant Markov chain. Accordingly, the fixed probability vector is given by the following equation:

$$Z = (Z_1, Z_2)$$

where

$$Z_2 = \frac{S_{12}}{S_{12} + S_{21}} = \frac{P}{P + Q} = t_2 \quad (2)$$

The bit correlation coefficient ζ is generally used frequently and defined as:

$$\zeta = 1 - P - Q \quad (3)$$

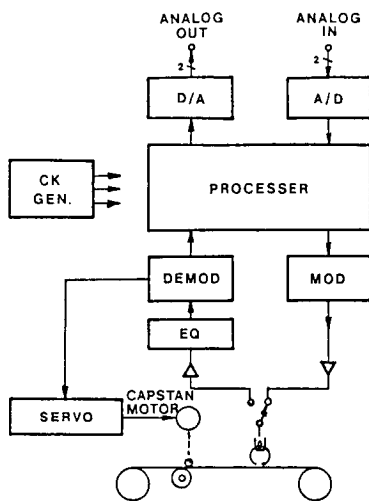


Fig. 7. Block diagram of digital signal processing.

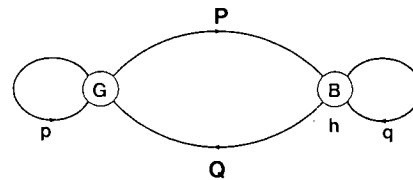


Fig. 9. Gilbert model.

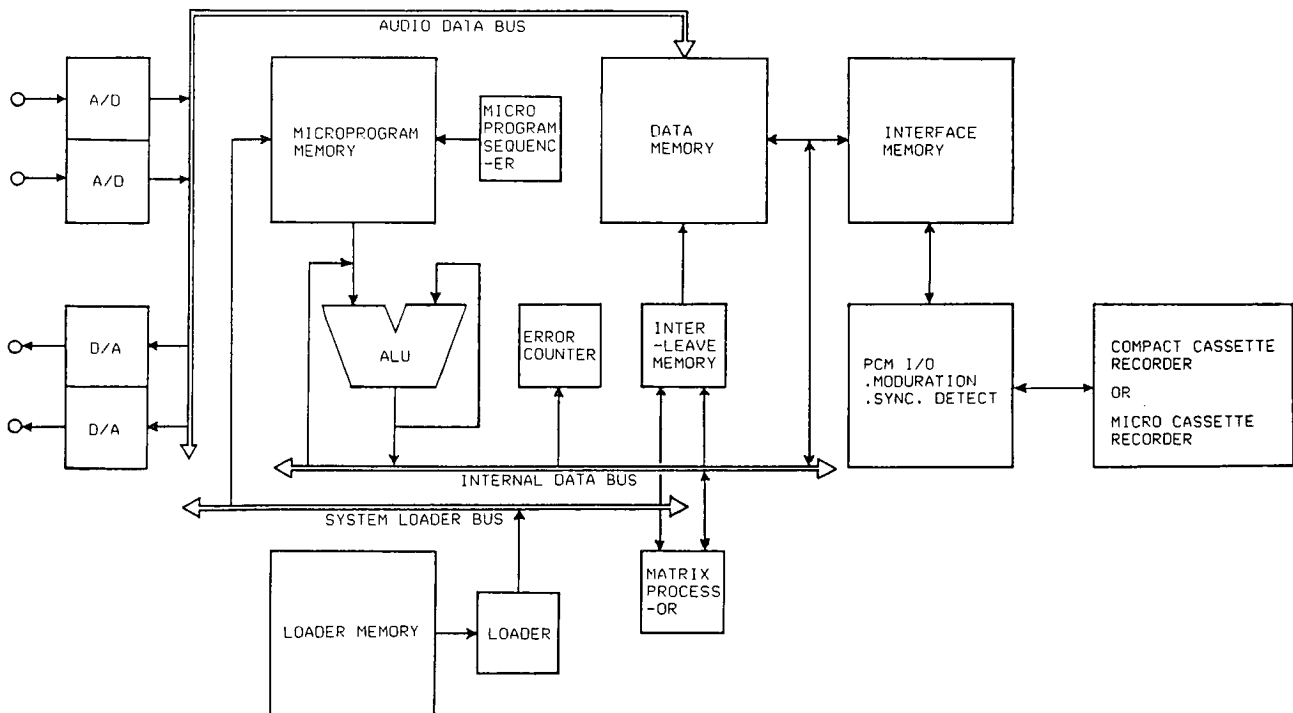


Fig. 8. Outline of universal processor.

ζ shows the nature of the code error with regard to burst or random characteristics. The code error tends more to burst error as ζ approaches 1 and tends more to random error as ζ approaches 0.

The probability $\text{Pr}(B)$ for an error in the n th bit after the burst is given by

$$\text{Pr}(B) = q^n + \sum_{i=2}^{n-1} i \cdot q^{i-1} \cdot p^{n-i-1} \cdot Q \cdot P \quad (4)$$

The probability t_2 of settling after time m from a burst generation is given by

$$t_2 = \frac{P}{P + Q} \quad (5)$$

(This gives the mean bit error ratio.)

The generation probability $P_i(s)$ for the continuous code error of i bits is given by

$$P_i(s) = Z_1 \cdot S_{12} \cdot S_{22}^{i-1} \cdot S_{21} \quad (6)$$

There are two methods to find the parameters.

1) To apply a nonlinear programming method so that the square of the difference between the run distribution

of theoretical code error calculated from $P_i(s)$ and the measured value is minimized.

2) To calculate the parameters from the following equations for mean burst length and mean nonerror burst length:

$$\text{mean burst length } \bar{B} = \frac{\sum_{i=1}^{\infty} N_i L_i}{\sum_{i=1}^{\infty} N_i} = \frac{1}{Q} \quad (7)$$

$$\begin{aligned} \text{mean nonerror burst length } \bar{G} &= \frac{(N - \sum_{i=1}^{\infty} N_i L_i)}{\sum_{i=1}^{\infty} N_i} \\ &= \frac{1}{P} \end{aligned} \quad (8)$$

where

L_i = average burst bit length the burst length distribution of which is in the interval of (l_{i-1}, l_i) bit

N_i = number of times the burst occurs

N = total number of bits within total time of observation.

Fig. 10 shows a measured example of the run dis-

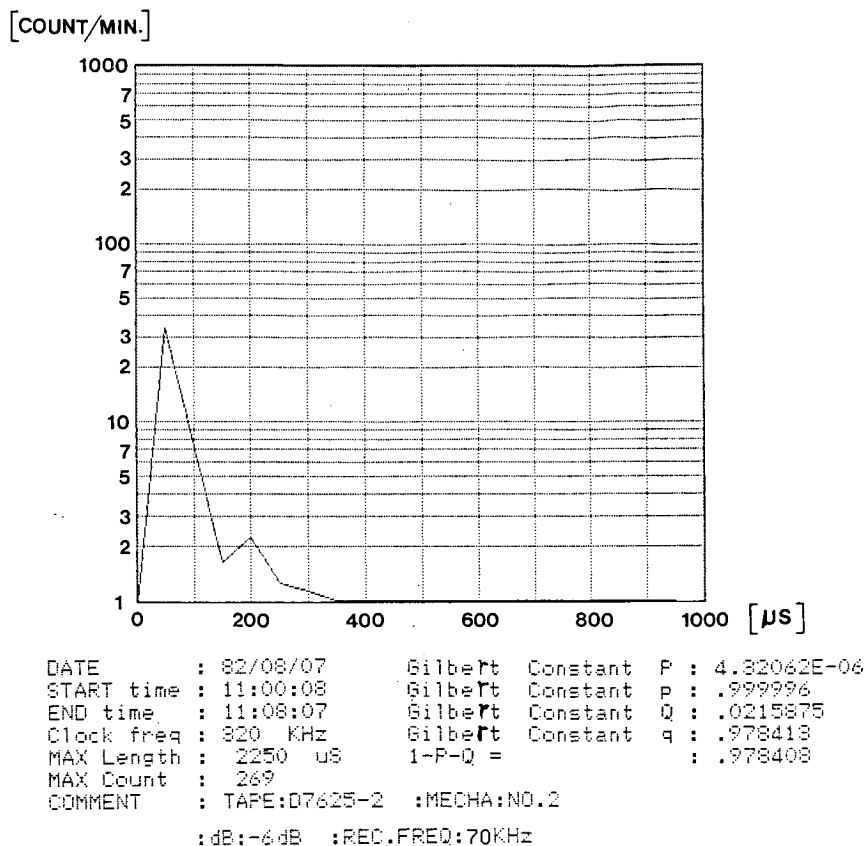


Fig. 10. Example of dropout run distribution of compact cassette digital recorder.

tribution of the dropout of the compact-cassette recorder, and Fig. 11 is a sketch of the dropout measuring system.

In this example the parameters of the Gilbert model are obtained from Eqs. (7) and (8) as follows:

$$Q = 0.216 \times 10^{-1}$$

$$q = 1 - Q = 0.978$$

$$p = 0.9999996$$

$$P = 1 - p = 0.432 \times 10^{-6}$$

Fig. 12 shows the generation probability $Pr(B)$ of error of the n th bit after the generation of a burst error calculated from the above parameters.

From the drawing the settling time m to the mean bit error ratio, $t_2 = P/(P + Q)$, is 2.83 ms.

The maximum burst length obtained from Fig. 10 is

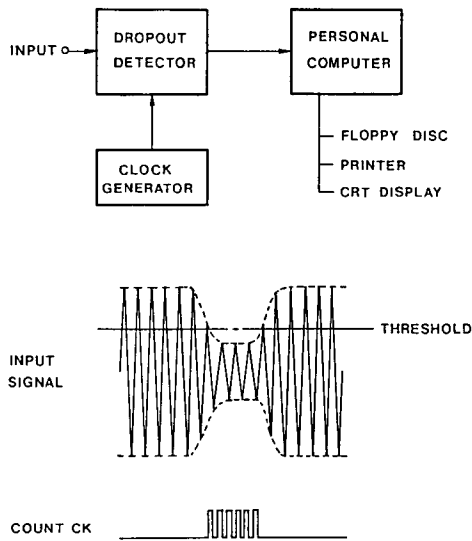


Fig. 11. Dropout measuring system.

2.25 ms. Accordingly the required interleave time in the tape longitudinal direction is 2.8 ms and higher, which is equivalent to three frames.

From the run distribution of Fig. 10,

$$\zeta = 1 - P - Q = 0.9784$$

and this indicates a high burst performance. Fig. 13 shows an example of the signal format now used.

8 PRACTICAL METHOD OF CODE ERROR CORRECTION

To ensure a high correction capability, the b-adjacent code is used for the correction of two error words. The inspection bits with the b-adjacent code are obtained

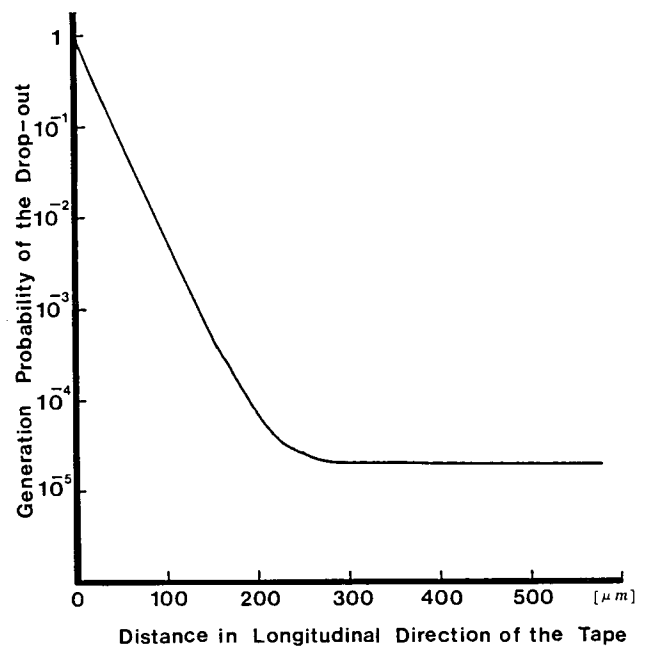


Fig. 12. Probability $Pr(B)$ of error of n th bit after generation of burst.

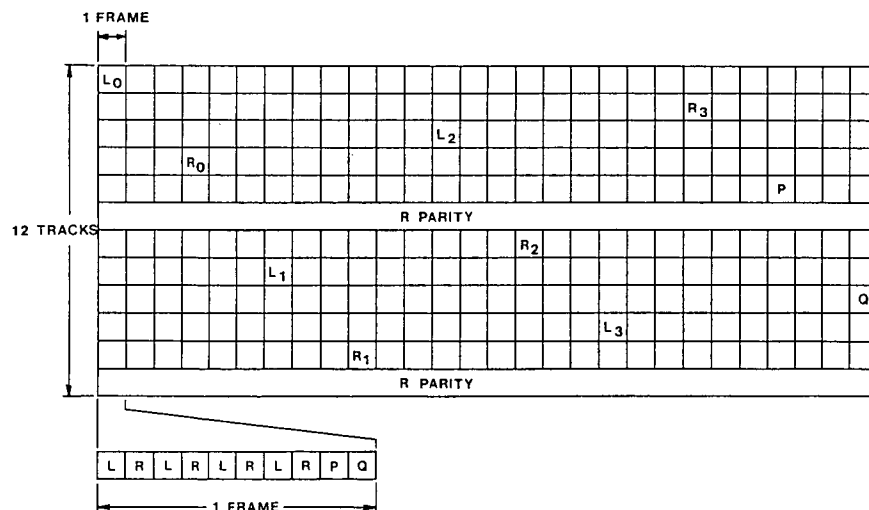


Fig. 13. Word sequence on tape of compact cassette digital tape recorder.

10 PROBLEMS TO BE SOLVED AND FUTURE DEVELOPMENT

The experimental recorders still have some problems to be solved.

- 1) The tape transport system is not stable, and the code error ratio fluctuates substantially. Problems are tape tension, tape slipping, and tape position control.
- 2) Influence of the cassette itself.
- 3) Servo by an exclusive track to prevent the influence of dropout.
- 4) Compatibility among decks.
- 5) Achievement of fewer tracks and shorter wavelength recording with the bulk head to reduce expensive multitrack circuit cost.
- 6) Recording and reproduction by a thin-film head having a potential of higher area density (20 Mbit/in²).

11 CONCLUSION

- 1) High-density recording and reproducing was realized with a comparatively small number of tracks, with a possibility of future circuit cost reduction.
- 2) A new error-correction system was developed which can correct the major dropout in any one of five tracks by combining parity in the tape-track direction, interleave, b-adjacent code, and CRCC.
- 3) Digital modulation systems, called FEM-4 and FEM-5, were developed to realize high packing density.
- 4) A signal processor of microprogramming capability was developed in which signal format, interleave length, and data arrangement can be changed and the error-correction codes can be selected for effective study of the system.

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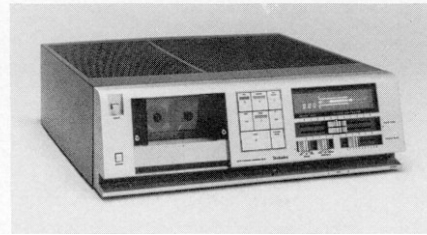


Fig. 15. Compact cassette digital tape recorder.



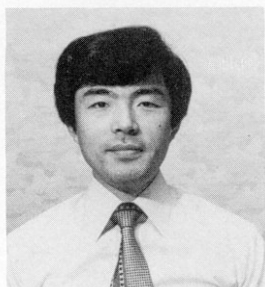
Fig. 16. Microcassette digital tape recorder.

the head; and Mr. Hanakawa, Chief Engineer and project leader, and also Mr. Kitakawa, Mr. Murai, Engineer, Mr. Nakamura, Mr. Shimada, Mr. Takizawa, Mr. Iwakuni, and Miss Tamaki, the group members, and all other persons concerned.

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The biographies of Messrs. Sakamoto and Kogure appear on pp. 645-646.