

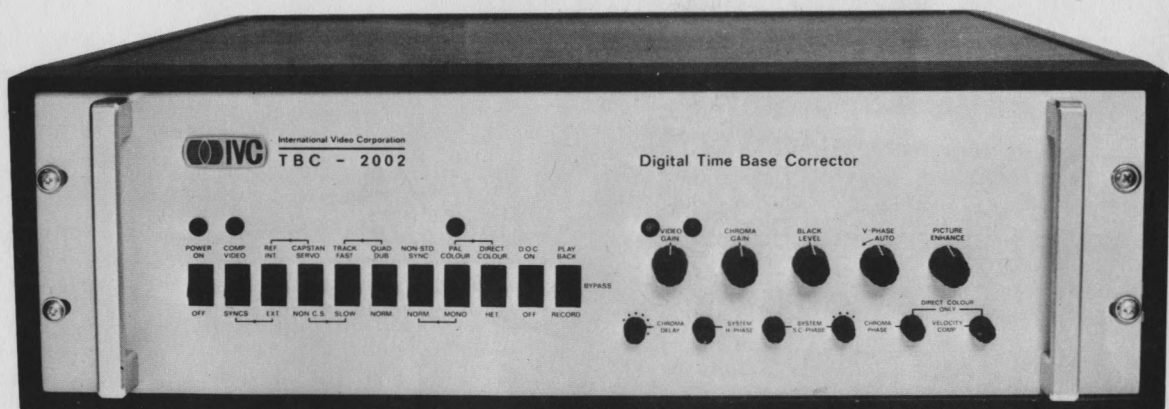
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International Video Corporation

IVC-TBC 2002

Digital Time Base Corrector Operators And Service Manual



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IVC TBC-2002

This manual is laid out in sections as shown below. A detailed breakdown for each section and its various sub-sections is contained on the first page of each section.

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GENERAL DESCRIPTION

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SECTION 1

GENERAL DESCRIPTION

1.1 DESCRIPTION AND PURPOSE

The IVC TBC-2002 Digital Time Base Corrector is designed for use with any helical scan video tape recorder. Playback video is processed line by line to remove time base errors and provides a synchronous output suitable for mixing, fading and special effects. The improvement provided by the editing capability of the unit results in smooth transitions of the edited scene. Though designed primarily for PAL colour applications, the unit may also be used with monochrome signals, (for SECAM see appropriate appendix).

Standard features include full video enhancement and noise reduction, 4 line store, capstan or non-capstan servo operation, and chrominance/luminance delay correction.

1.2 AVAILABLE OPTIONS

16H Window: In situations where extremely large time base errors are encountered, the standard 4H window may be replaced by the 16H window option. This increases the storage capacity to 16 horizontal lines and provides an error correction window of ± 8 lines. To introduce this option it is merely necessary to replace the standard 4H Store card with the 16H Store card.

Quad Dub: When operating with a non-capstan servo or remote VTR, this option provides a correctly related PAL colour output that can be dubbed onto a wideband, direct-record VTR. When required, this card is fitted above the Output Filter card which contains three mounting pillars for the purpose. This feature is not necessary for capstan servo VTRs.

Carrying Case: If the TBC-2002 is to be used in portable applications, a 19-inch carrying case is available.

1.3 DIGITAL TIME BASE CORRECTION

The TBC-2002 uses digital techniques to

perform time base correction. The off tape signal is converted into a sequence of digital data words representing successive picture elements which are written into, and read from, the store memory at different clock rates. Input data words are written into memory by a clock that is locked to off tape horizontal sync pulses. Output data words are subsequently read from the memory by a stable clock that is locked to the internal sync pulse generator. The irregular input signal is thus stabilised and timing errors removed.

The sync pulse generator may in turn be locked to local station sync pulses, an external composite video signal, its own internal precision reference oscillator or, in the case of non-capstan servo VTRs, to the average off tape field frequency.

The standard TBC-2002 has a memory capacity of four horizontal lines. Through the use of high speed random access devices, this memory capacity provides a time base error correction window of four horizontal lines which is more than adequate for timing errors normally encountered in helical VTR outputs. The TBC-2002 includes a picture enhancer/noise reducer feature which provides an adjustable degree of enhancement when operating with narrow band colour VTRs.

A further level of correction to the input signal is provided by an oxide drop-out compensator which re-inserts a correctly timed colour signal from a previous location in the memory. The compensator requires a signal from the VTR to indicate the presence of a drop-out. This signal is available on many machines, either as the RF level at the read-head pre-amplifier, or as a TTL pulse which is provided to indicate drop-out. A high impedance DOC input is provided at the TBC-2002 to allow ready connection of the RF envelope, or a TTL pulse.

A full video processing amplifier at the output of the TBC-2002 ensures that the digitally corrected output complies with broadcast specifications.

TABLE 1.1
TBC-2002 SPECIFICATION

Video Signal Performance

Input Video	625/50 Monochrome or PAL heterodyned colour from non-segmented helical VTRs, with or without capstan servo.
Input Level	1V $\pm$ 3dB composite video into 75ohms
Input Impedance	75ohms. Return loss better than 30dB to 5MHz.
Output Video	Two composite outputs at standard level.
Output Impedance	75ohms. Return loss better than 30dB to 5MHz.
Bandwidth (Monochrome)	5.5MHz, -3dB
Bandwidth (Colour)	3MHz, -3dB in luminance path
K-Factor (2T pulse)	2% Monochrome, 4% Colour
Differential Phase	3°
Differential Gain	3%
Signal-to-Noise Ratio	54dB peak signal to r.m.s. noise
Chroma Gain Range	$\pm$ 6dB
Picture Enhancer	Enhancement and noise coring of luminance components in frequency band 1.5MHz - 3MHz. Enhancement range 6dB. Coring level internally preset. Bypass provided.

Processing Amplifier

Video Blanking	Output signal blanked with controlled rise and fall times to remove input syncs and colour burst.
Syncs and Colour Burst	Reinserted at standard level from gen-lockable internal Sync Generator.

Time Base Correction

Correction Window	4 horizontal lines in full colour framed edit mode. Store option provides 16H window for larger errors.
Corrected Stability	Chrominance 4ns, Luminance 40ns (Sig/Noise 40dB or more).

Sync Generator

Reference Input (Capstan Servo Mode)	Composite Sync, subcarrier, and PAL ident (3 wire) Composite video (1 wire) at standard levels.
Pulse Outputs	Composite sync, composite blanking, H drive, V drive, burst flag and DIN PAL ident at 2 volts into 75 Ω . Squarewave PAL ident available at 1 volt into 75 Ω .

TABLE 1.1
TBC-2002 SPECIFICATION (continued)

Subcarrier	Correctly related subcarrier at 1 volt p-p into 75Ω in capstan servo mode. Also available in non-capstan servo mode (as option) for dubbing to quad with non-capstan servo or remote VTRs.
Advanced VTR Sync	Advanced pseudo composite sync at 2 volts into 75Ω , with manual adjustment over 20 lines for V-locked capstan servo VTRs. In 'Auto' mode an advance of 2H (8H with 16H store option) is automatically maintained – dynamically centres TBC window.
Physical	
Size	5.25" (133mm) high x 19" (482mm) wide x 19.1" (485mm) deep.
Weight	26lbs (11.8kg)
Power	100VA approx. 220/240V – 50/60Hz
Ambient Temperature	10°C to 40°C operating

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FIGURE 2.1 TYPICAL CONNECTION FOR
CAPSTAN SERVO, ONE WIRE
GEN-LOCK

FIGURE 2.2 TYPICAL CONNECTION FOR
CAPSTAN SERVO, THREE WIRE
DRIVE OR ONE WIRE
MONOCHROME

FIGURE 2.3 TYPICAL CONNECTION FOR
NON CAPSTAN SERVO

SECTION 2 INSTALLATION AND SET-UP

2.1 GENERAL

The IVC TBC-2002 Time Base Corrector is designed for either portable or rack-mounted use. When used in portable applications, the unit may be bolted into a standard 19-inch carrying case, supplied as an option.

When the unit is mounted in a standard rack, vertical space of 5¼ inches is required. In addition to the allowance of 19¼ inches for the depth of the TBC-2002, sufficient space is required at the rear unit for cable connections and ventilation. Cooling air must not be prevented from exhausting freely from both sides of the TBC-2002.

When mounting the unit in an equipment rack, it is necessary to provide rear support or to use rack sliders which are available as an option. The unit must NOT be only supported by the front panel.

If no clearance is available below the unit the feet must be removed from the bottom cover.

Under NO circumstances may the unit be permanently installed with top and bottom covers removed as the ventilation flow will be seriously impaired.

2.2 UNPACKING AND REPACKING

2.2.1 Unpacking

Carefully unpack the equipment, and, before discarding the packing material, check to determine if the unit is complete and with all ordered accessories.

Inspect items for evidence of shipping damage. If there is evidence of any such damage, notify the carrier of the nature of the damage and arrange to have the shipment inspected by the carrier's agent or authorised representative. Do not delay. Inform the carrier of intent to file a claim and notify your IVC office or representative immediately.

2.2.2 Packing

If at all possible, retain the original shipping carton and preformed packaging material for reshipment.

To protect the TBC-2002 against the normal hazards of shipping, use the best methods and best packaging materials available. Since the power supply unit is mounted in the right hand rear corner of the unit, adequate support must be provided in this region to prevent distortion of the cabinet. If original materials are unavailable or are not re-usable, pack the TBC-2002 as follows:

a) Use a double-walled carton that meets the shipping carton test strength indicated below:—

GROSS WEIGHT	CARTON TEST STRENGTH
Up to 10lbs (4.5kg)	200lbs (90.5kg)
10–30lbs (4.5–13.5kg)	275lbs (124.5kg)
30–120lbs (13.5–54.5kg)	350lbs (158.5kg)
120–140lbs (54.5–63.5kg)	500lbs (226.5kg)
140–160lbs (63.5–72.5kg)	600lbs (272.0kg)

b) Protect all surfaces with heavy paper, plastic or sheets of cardboard. Use non-abrasive materials such as foam rubber or soft cushioning paper around all projecting parts.

c) Pack at least 4 inches (10cm) of industry-approved, shock-absorbing material around the top, bottom and each side of the unit.

d) Secure the outside of the carton with heavy duty shipping tape. Mark each side of the shipping carton as follows:—

FRAGILE – HANDLE WITH CARE

2.3 POWER REQUIREMENTS

The IVC TBC-2002 must be ordered to operate from either 110/120V or 220/240V ac power input, and with frequencies of 48Hz to 63Hz. Line voltage variations of 198V to 264V (99V to 132V) can be tolerated.

The TBC is supplied with a 3-conductor power cable, one end of which connects to the 3-pin IEC POWER-IN plug on the rear panel of the unit. The free cable end must be wired according to the following colour code:—

Brown — LINE
Blue — NEUTRAL
Green/Yellow — EARTH

2.4 SET UP-PROCEDURE

The following procedure serves to check the IVC TBC-2002 printed circuit cards prior to operation.

1. Connect a broadcast standard colour bar signal from the station or from a suitable fully interlaced test signal generator to the COMP VIDEO reference input on the TBC-2002 rear panel. (For monochrome applications, use a multi-burst test signal).

2. Connect a co-axial jumper between the remaining COMP VIDEO loop through connector and the VIDEO IN connector.

3. Connect the VIDEO OUT main connector on the rear panel to a picture monitor via a vector-scope. Terminate the remaining loopthrough connectors with 75 ohms.

4. Select the required mode of operation on the front panel selector switches:—

PAL COLOUR or MONO
HET (if in colour mode)
EXT (reference)
COMP VIDEO
NORM (syncs)
CAPSTAN SERVO
PLAYBACK

5. Set the VIDEO GAIN, CHROMA GAIN and BLACK LEVEL controls on the front panel at the unity position (i.e. the engraved lines pointing upwards).

6. Set the V-PHASE control on the front panel to the AUTO position (i.e. fully anticlockwise).

7. Set the PICTURE ENHANCE control on the front panel fully anticlockwise, (i.e. the OFF position).

8. Turn on the signal generator and monitoring equipment, and press the POWER ON switch on the TBC-2002.

9. Check that the fan is operating. Under no circumstances must the TBC-2002 be allowed to operate if the fan is not working.

10. With an oscilloscope, verify the presence of appropriate signals at the INTERNAL SYNC GEN OUTPUTS and VTR LOCK BNC connectors on the rear panel.

11. Check that the TBC-2002 video output is locked vertically and horizontally to the input. Vertical phasing is 2 lines delayed due to delay through the TBC-2002 (8 lines delayed if the 16H Store option is used).

12. With the vectorscope subcarrier selections set to EXT, and with a reference subcarrier feed from the generator (NOT the TBC), verify operation of the system subcarrier phase controls on the front panel.

13. Select BYPASS on the front panel and check that the monitor shows unprocessed colour bar test pattern.

14. Switch off the TBC-2002 and disconnect the colour bar test pattern and monitoring equipment.

The equipment is ready to be set up for the required operating configuration.

2.5 TYPICAL CONNECTIONS

In order to assist understanding of connections into a TV system, three sample connection schematics are shown on Figures 2.1, 2.2 and 2.3. A description of the rear panel connections is given in Section 3.

Figure 2.1: Capstan Servo, One Wire Gen-Lock

This is a typical professional use of the TBC-2002 and Capstan Servo VTR to provide a fully synchronous output. The Gen-Lock input may be Colour Black, Colour Bars or Station Video. It may even be an off-air feed. The SPG outputs will be fully related to this Gen-Lock input and may be used to drive other studio equipment.

Figure 2.2: Capstan Servo, Three Wire Sync Drive

This provides the same facilities as in Figure 2.1 but would be used when the TBC-2002 is to be permanently wired into a Studio System.

Figure 2.3: Non Capstan Servo

In the non capstan servo mode it is not necessary to provide reference inputs as the internal SPG becomes related to the mean off-tape vertical frequency. The reference inputs may however be left connected as the SPG will ignore these when switched to non capstan servo. The SPG outputs will also follow the TBC-2002 output and may still be used to drive other studio equipment which will then be synchronous to the connected output. Note that in this mode only the colour signal will be unrelated to fH.

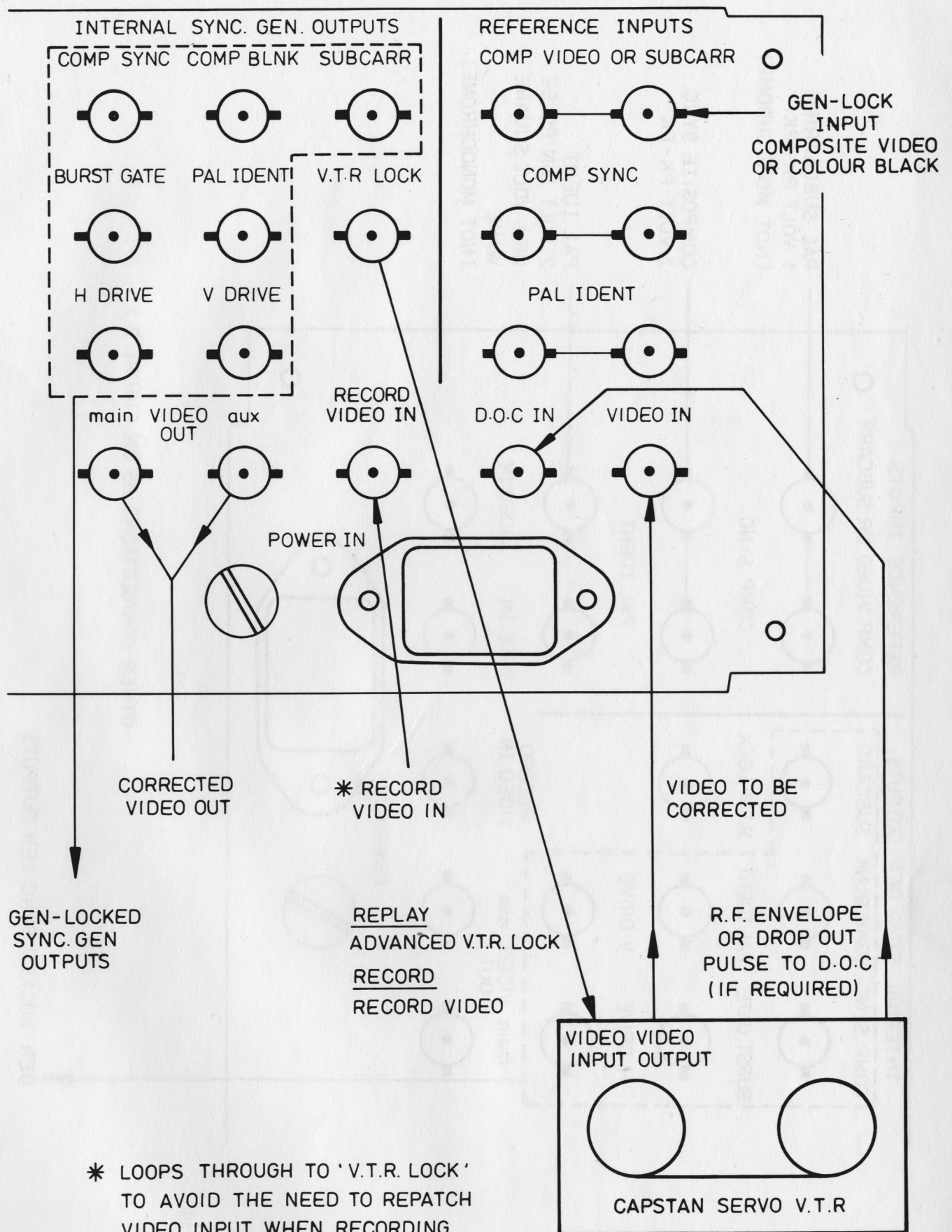
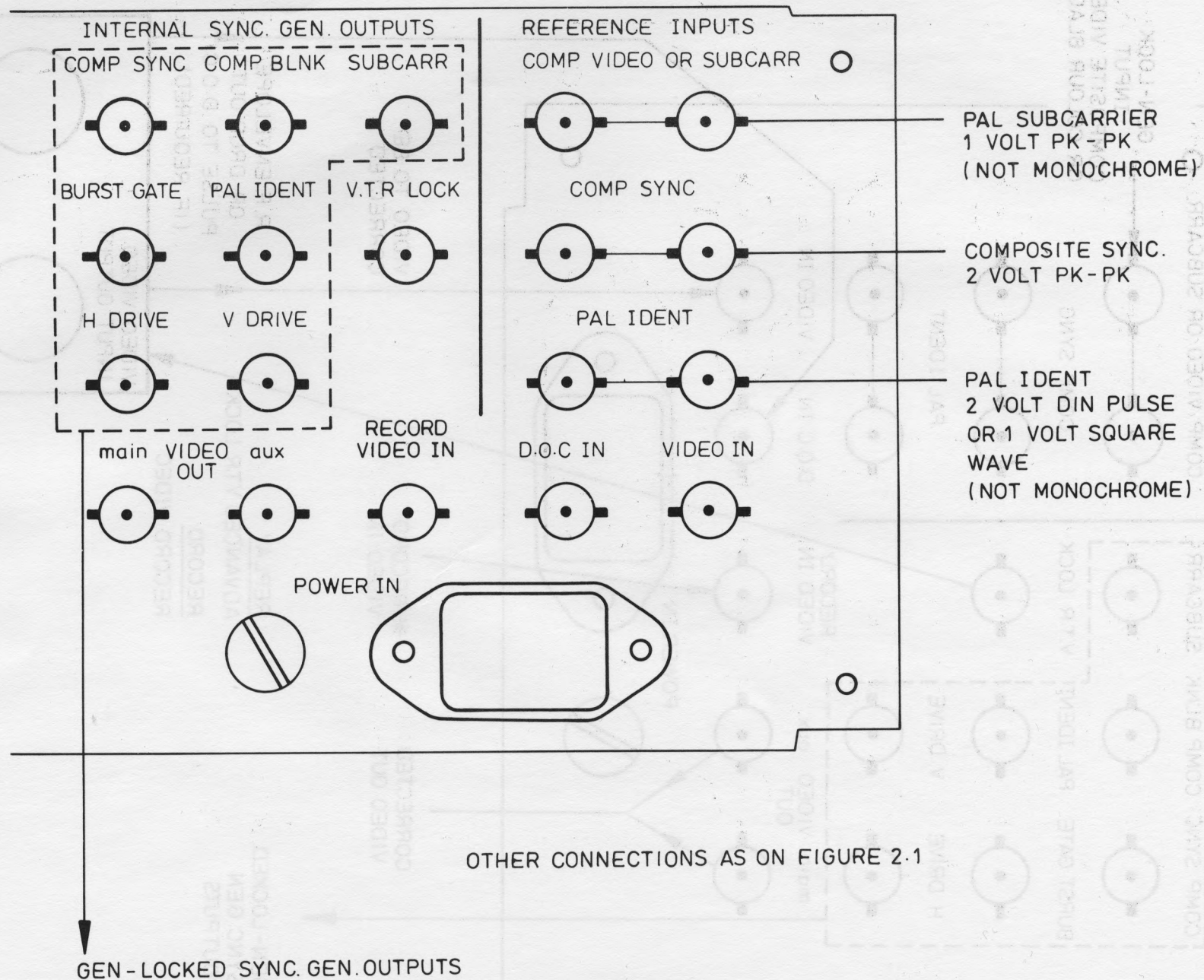


FIGURE 2.1 TYPICAL CONNECTION FOR CAPSTAN SERVO, ONE WIRE GEN-LOCK

FIGURE 2.2 TYPICAL CONNECTION FOR CAPSTAN SERVO,
THREE WIRE DRIVE OR ONE WIRE MONOCHROME



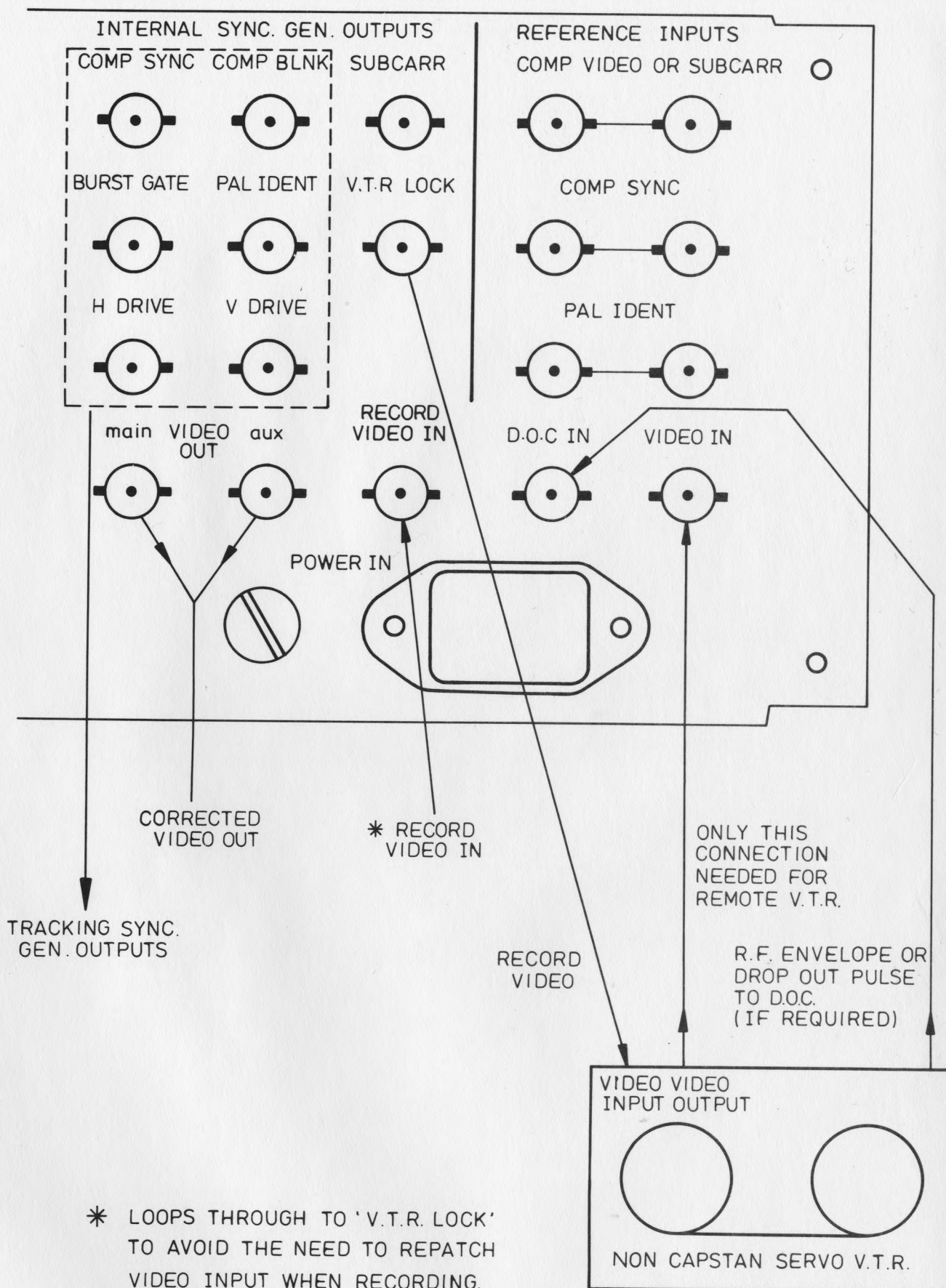


FIGURE 2.3 TYPICAL CONNECTION FOR NON-CAPSTAN SERVO

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FIGURE 3.1 TBC-2002 FRONT PANEL

FIGURE 3.2 TBC-2002 REAR PANEL

SECTION 3 OPERATION

3.1 FRONT PANEL SELECTOR SWITCHES

SWITCH POSITION	FUNCTION
a) PLAYBACK/BYPASS/RECORD selector switch	
PLAYBACK	This is the normal operating condition. The position is selected for replay mode where the video output from the VTR provides the VIDEO IN signal to the TBC-2002 for correction. An advanced sync signal from the TBC-2002 is routed via the VTR LOCK connector on the rear panel to the video input on the VTR.
BYPASS	When this position is selected, the VIDEO IN signal is routed directly to the main VIDEO OUT connector on the rear panel. The advanced sync signal is still fed to the VTR to maintain lock, and the corrected signal is available at the aux video output.
RECORD	In this position the TBC-2002 is inoperative. The RECORD VIDEO IN signal is connected to the VTR video input via the VTR LOCK connector to avoid the need to repatch the video input when recording. The VTR locks up to the signal being recorded.
b) PAL COLOUR/MONO selector switch	
PAL COLOUR	The TBC-2002 selects the video mode for processing PAL colour signals. The green LED above lights up when the input video has a PAL colour burst.
MONO	The TBC-2002 selects the non-colour processing mode which provides a full bandwidth for monochrome only replay.
c) DIRECT COLOUR/HET selector switch	
Effective only when PAL COLOUR is selected.	

SWITCH POSITION	FUNCTION
DIRECT COLOUR	The TBC-2002 handles direct colour input from wideband helical VTRs, when the appropriate option is fitted.
HET	Allows the TBC-2002 to handle colour under as hetrodyned colour output from helical VTRs and VCRs.
d) NON STD SYNC/NORM selector switch	
NON STD SYNC	Selected if the input signal has non standard back porch for reference black level.
NORM	Selected for normal sync operation
c) DOC ON/OFF selector switch	
DOC ON	Reinserts full colour signal from RAM store at the time of a tape drop out. The appropriate connections must be made to the DOC IN connector on the rear panel for the switch to function. If no connection is made, the TBC-2002 will malfunction if the switch is operated.
OFF	Inhibits the drop out compensation circuits.
f) CAPSTAN SERVO/NON CS selector switch	
CAPSTAN SERVO	The TBC-2002 provides advanced syncs to V-lock a capstan servo VTR. The TBC-2002 output is fully synchronous.
NON CS	The TBC-2002 V-locks to video from a non-capstan servo or remote VTR. The unit removes time base errors from the replay signal but the SPG master frequency becomes related to the mean off tape vertical frequency.
g) TRACK FAST/SLOW selector switch	
Effective only when NON CS is selected	
TRACK FAST	Selects fast tracking rate to handle large, rapid time base errors from very simple non-capstan servo VTRs.
SLOW	Normal non-capstan servo operation.
h) QUAD DUB/NORM selector switch	
QUAD DUB	When NON CS is selected and the Quad Dub option is incorporated, correctly related chrominance is provided to allow dubbing to direct record type VTRs.
NORM	Provides stable, but unrelated, chrominance output for direct viewing, CCTV or CATV, applications from

CONTROL	FUNCTION
BLACK LEVEL	Adjusts the black level of the signal over the range $\pm 15\%$. This control is also unity calibrated.
V-PHASE	In CAPSTAN SERVO mode, provides control of vertical picture position relative to output vertical blanking. The fully anti clockwise position (AUTO) provides automatic phasing of VTR LOCK signal to maintain dynamic centring of the TBC window.
PICTURE ENHANCE	Controls amount of enhancement applied. Bypassing the enhancer circuit in the fully anti clockwise (OFF) position.
CHROMA DELAY	Adjusts relative chrominance/luminance delay over the range +250ns to -100ns in 50ns switched steps.
SYSTEM H PHASE	With external reference mode selected, adjusts H-phasing of the TBC-2002 output relative to the gen-lock reference.
SYSTEM SC PHASE	Fine and coarse controls which adjust the subcarrier phasing of the TBC-2002 output relative to locking input in external reference mode.
(Fine control)	Continuous control of phase over not less than 90° .
(Coarse control)	Four switched steps of 90° .
CHROMA PHASE	Applicable to connection of direct colour replay signals only. Corrects burst-to-picture phase to minimise colour errors.
VELOCITY COMP	Applicable to correction of direct colour replay signals only. Optimises compensation of velocity errors.

3.3 REAR PANEL CONNECTIONS

CONNECTOR	FUNCTION
INTERNAL SYNC GEN OUTPUTS: COMP SYNC, COMP BLANKING, SUBCARRIER, BURST GATE, PAL IDENT, H DRIVE, V DRIVE	These SPG outputs are fully standard CCIR format. They will be either "stand alone", tracking or locked to reference depending upon the mode selected.
VTR LOCK	Provides advanced VTR LOCK signal to the capstan servo VTR. In RECORD mode, provides the record video signal to the VTR input.
RECORD VIDEO IN	In RECORD mode, loops through to VTR LOCK for connection to VTR input to avoid the need to repatch the video input when in PLAYBACK mode.

SWITCH POSITION	FUNCTION
NORM (cont)	non-capstan servo VTRs. For capstan servo VTRs, the output is always fully synchronous and this switch is irrelevant.
j) REF INT/EXT selector switch	
Effective only when CAPSTAN SERVO is selected.	
REF INT.	The TBC-2002 internal sync generator locks to internal precision reference oscillator, and becomes a broadcast standard SPG.
EXT.	The TBC-2002 internal sync generator locks to external reference.
k) COMP VIDEO/SYNCS selector switch	
Effective only when CAPSTAN SERVO is selected.	
COMP VIDEO	The TBC-2002 sync generator gen-locks to composite video (one wire locking). The green LED above lights up to indicate PAL burst is present on the gen-lock input.
SYNCS	The TBC-2002 sync generator gen-locks to composite sync, subcarrier and PAL ident (3 wire locking).
l) POWER ON/OFF selector switch	
POWER ON	Connects mains power to the TBC-2002. Red LED above lights up to indicate the TBC-2002 is operative.

3.2 FRONT PANEL VARIABLE CONTROLS

CONTROL	FUNCTION
VIDEO GAIN	Adjusts VIDEO IN amplitude over the range of $\pm 3\text{dB}$. The control is calibrated to provide unity gain with a normal IV composite signal.
Green LED	Indicates VIDEO IN signal has sufficient amplitude.
Red LED	Illuminates when VIDEO IN luminance peaks exceed correct amplitude.
	Note: These LED indicators are provided for field use where full monitoring equipment is not available.
CHROMA GAIN	Adjusts the saturation of the colour signal over the range zero to $+3\text{dB}$. This control is also unity calibrated.

CONNECTOR	FUNCTION
VIDEO IN	Video from VTR which is TO BE CORRECTED.
VIDEO OUT	The main VIDEO OUT signal follows the mode selected. The auxiliary VIDEO OUT signal is always connected.
DOC IN	Connects RF envelope or drop-out pulse (if applicable) to the drop-out compensator circuits.
REFERENCE INPUTS:	These inputs must be terminated in 75 ohms if not looped through.
COMP VIDEO or SUBCARRIER	Input of composite video or "Colour Black" reference feed for one wire gen-lock (external comp video lock) OR Input of subcarrier in external sync three wire lock.
COMP SYNC	Input of composite syncs in external sync three wire lock.
PAL IDENT	Input of PAL IDENT in external sync three wire lock. (Either IV 7.8kHz square wave or DIN pulse).
POWER IN	Live input, either 220/240V 50Hz or 110/120V 60Hz (as ordered).

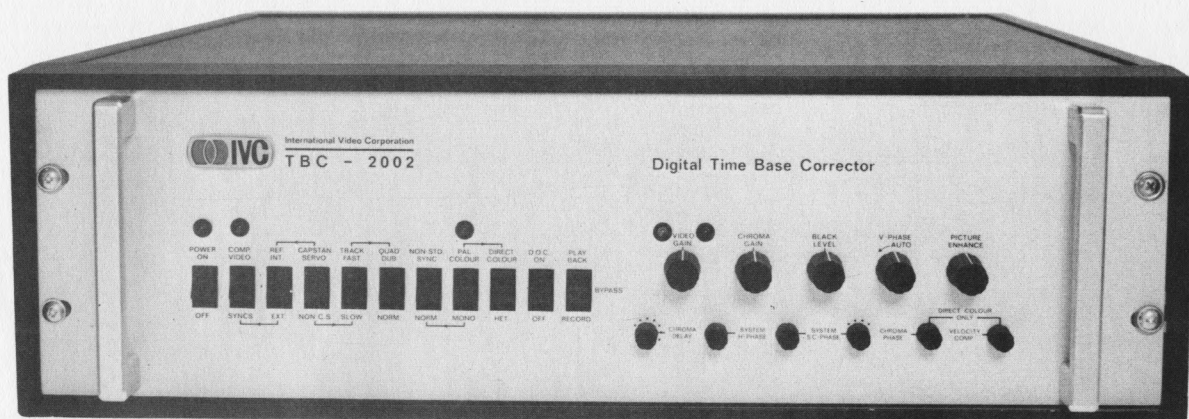


FIGURE 3.1 TBC-2002 FRONT PANEL

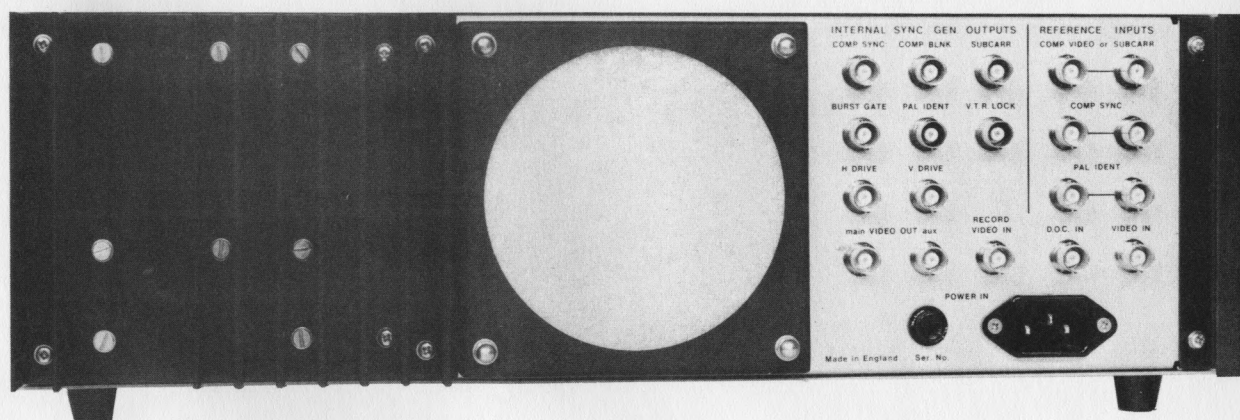


FIGURE 3.2 TBC-2002 REAR PANEL

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FIGURE 4.1 TBC-2002 BLOCK DIAGRAM

SECTION 4

SYSTEM DESCRIPTION

4.1 GENERAL

The IVC TBC-2002 corrects an input signal from a helical scan video tape recorder, and, when operating in the capstan servo mode, one of the following three references is used:—

- a) External composite video
- b) Composite sync, PAL ident, subcarrier
- c) Internal crystal reference

A VTR LOCK feed from the TBC-2002 to a capstan servo VTR establishes the correct vertical phasing automatically. A V PHASE manual control is also provided on the front panel. If the VTR is capable of supplying playback RF envelope, or a negative active TTL pulse from a drop-out detector, then the full use of the digital drop-out compensator circuitry (DOC) in the TBC-2002 will enhance the quality of the processed video output.

4.2 PRINCIPLES OF OPERATION

The VTR output fed to the VIDEO IN connector on the rear panel of the TBC-2002 is routed directly to the NORMAL/BYPASS relay on the Input Processor card. With BYPASS selected on the front panel, the video signal passes, via a further NORMAL/BYPASS relay on the Output Processor card, to the main VIDEO OUT connector on the rear panel.

With PLAYBACK selected on the front panel, the video signal is terminated in 75 ohms on the Input Processor card. The front panel VIDEO GAIN control allows a range of $\pm 3\text{dB}$ variation. When set at unity position, an input level of 1V peak-to-peak gives an output level of 1V peak-to-peak providing the TBC-2002 is correctly aligned.

With normal syncs (i.e. the NON STD SYNC/NORM selector switch on the front panel is in the NORM position) the video signal is accurately clamped with black level at or near 0V as determined by adjustment of the front panel BLACK LEVEL control. The signal is applied to a high input impedance buffer amplifier which drives both the precision sync separator, for normal applications, and the non-standard sync separator, for applications where NON STD SYNC is selected on the front panel.

In the BYPASS mode, a further output from the buffer amplifier is routed to the input of the clamp amplifier so that the TBC-2002 remains locked to the off-tape video and continues to operate normally. This facility ensures that time base corrected video is instantly available at the main VIDEO OUT connector when switching from BYPASS to PLAYBACK, and also provides an auxiliary VIDEO OUT signal in BYPASS mode. In the event of a power failure, the TBC-2002 automatically switches to BYPASS mode in which case the auxiliary VIDEO OUT connector is ineffective.

Clamped video is routed via the Input Filter and Input Oscillator cards to the luminance analogue-to-digital converter (ADC) card. A further output from the clamp amplifier feeds chrominance to the saturation control device and to the optional Direct Record card connector. The clamped video also feeds a sync amplitude detector circuit which drives the green LED on the front panel. This LED is a low amplitude syncs indicator, (on when level is adequate).

The chrominance from the clamp amplifier may be adjusted by the CHROMA GAIN control on the front panel and passes through a tapped chroma delay line to the PAL demodulator. Eight selectable delay positions provide front panel correction (via the CHROMA DELAY control) for

chrominance/luminance delay errors. Demodulated colour difference signals from the Input Processor card are routed to the chrominance ADC card via 1.5MHz low pass filters and the chrominance multiplexer on the Input Oscillator card.

The Input Filter card contains two low pass filters, one with a bandwidth of 5.5MHz for monochrome mode, and the other with a bandwidth of 3MHz for colour mode. The filtered luminance signal is connected to the Input Oscillator card from where it is passed directly to the luminance ADC card. In the colour mode it is sampled at a 7.2MHz rate, and in the monochrome mode at a 14.4MHz rate.

On the chrominance ADC card, the two colour difference signals (R-Y, B-Y) are switched alternately at 3.6MHz to form a multiplexed colour difference signal which is sampled at a 7.2MHz rate.

Video data enters the Store card via a digital multiplexer as 8-bit words at a 14.4MHz rate. In monochrome mode, the digital multiplexer routes data presented at its luminance input port only, at the 14.4MHz rate from the luminance ADC. In colour mode, the luminance data input to the multiplexer reduces to a 7.2MHz rate and is interleaved at the multiplexer output with alternate samples of the colour difference signals from the chrominance ADC to form a multiplexed 14.4MHz luminance and chrominance data stream. The multiplexed output of 8-bit words at the 14.4MHz rate is demultiplexed to 24-bit words at 4.8MHz before entering the buffer store which has a capacity of four 24-bit words. This is sufficient to remove the asynchronism between the TBC-2002 input and output clocks. The 24-bit words leave

the buffer store and enter the main store at the TBC-2002 output clock rate. The off-tape data is written into the main store Random Access Memory devices (RAMs) line by line, and is subsequently retrieved from the same memory locations in sympathy with the TBC-2002 output line rate. The 24-bit words leaving the main store RAMs are multiplexed back to a 14.4MHz stream of 8-bit words before passing from the Store card to the Output Processor card.

In the monochrome mode, the 14.4MHz data entering the Output Processor card is latched and applied to a luminance digital-to-analogue converter (DAC) to reconstitute the full bandwidth monochrome signal. After blanking, the monochrome signal is routed via a 5.5MHz low pass filter on the Output Filter card, and returns to the Output Processor card for the addition of syncs.

In the colour mode, the 14.4MHz data entering the Output Processor card is digitally demultiplexed to separate the interleaved luminance and colour difference data which are converted to analogue form by three separate DACs. The luminance DAC now operates at 7.2MHz. After blanking, the luminance signal is routed through a 3MHz low pass filter on the Output Filter card to the Enhancer card before returning to the Output Processor card. The two chroma DACs provide the analogue colour difference signals which are resampled, blanked and low pass filtered before passing to the chroma modulators. The combined output of the modulators is bandpass filtered and delayed before being added with syncs to the luminance signal from the Enhancer card. A video amplifier finally buffers the composite signal and feeds the main and auxiliary VIDEO OUT connectors at 75 ohms.

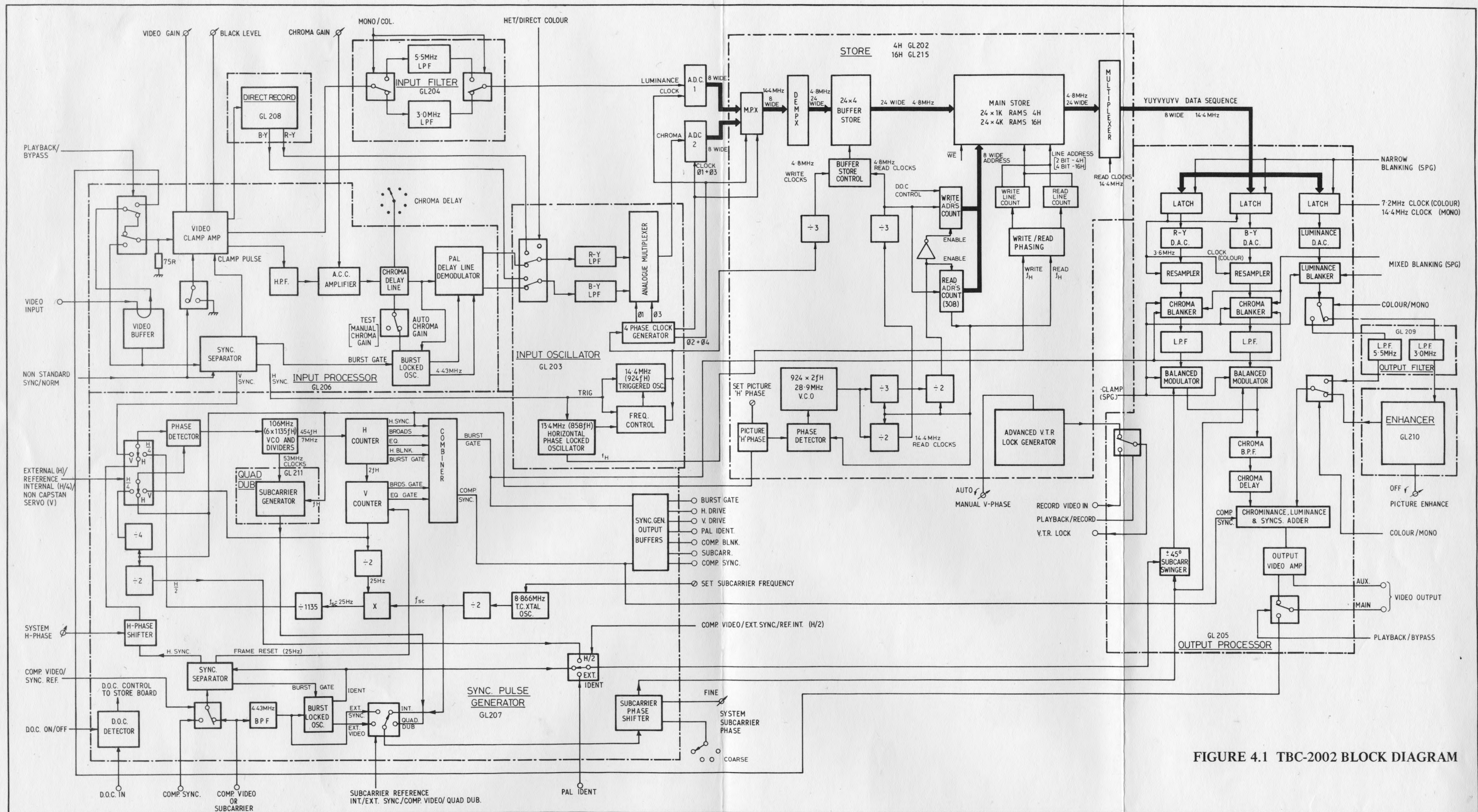


FIGURE 4.1 TBC-2002 BLOCK DIAGRAM

SECTION 5

SECTION 5 MAINTENANCE

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FIGURE 5.1 TBC-2002 BOTTOM VIEW

FIGURE 5.2 TBC-2002 TOP VIEW

FIGURE 5.3 PSU ASSEMBLY

SECTION 5 MAINTENANCE

5.1 MECHANICAL CONFIGURATION

The printed circuit cards are mounted horizontally above and below the centre chassis. Those cards containing input circuitry are mounted on the underside of the chassis as shown on Figure 5.1, and are listed as follows:—

Input Oscillator	GL203
Input Processor	GL206
Input Filter	GL204
2 x ADC PCB's	GL217

The switch panel (GL212) is also accessible from the underside of the chassis.

The 4H Store card GL202 (or 16H Store option GL215) is mounted immediately below the top cover and, with the two nylon clamps released, hinges open as shown on Figure 5.2 to allow access to the remaining output cards:—

Sync Pulse Generator	GL207
Output Processor	GL205
Output Filter	GL209
Enhancer	GL210

The Enhancer card is mounted on three nylon pillars above the Output Processor card. When the optional Quad Dub card (GL211) is used, it is located on three nylon pillars above the Output Filter card.

The Soft Start card (GL218), $\pm 15V$ Regulator card (GL216) and $-5.2V$ Regulator card (GL222) are housed on a mounting plate at the side of the power supply unit as shown on Figure 5.3.

This method of construction provides an even flow of ventilating air throughout all parts of the TBC-2002, whilst the centre chassis gives excellent isolation between the input and output asynchronous circuitry.

5.2 ACCESS

To gain access to the printed circuit cards and

power supply units, remove the top and bottom covers by loosening the captive DZUS fasteners, using the key (F3) provided.

When the TBC-2002 is rack-mounted, it is recommended that fully extending hinged rack slides are used so that the unit may be pulled clear of the rack for servicing. A suitable rack slider kit is available.

For stand-alone units, simultaneous access to input and output circuitry for maintenance purposes can be achieved by standing the TBC-2002 on its left side with top and bottom covers removed. In this position the Store card can be hinged down providing access to the output cards.

The printed circuit cards are held in place by nylon pillars. To remove any card, ensure all connectors are disconnected and release the nylon clamps. The Store card is attached to the hinge bar by M2.5 screws.

If it is necessary to gain access to the front panel components, first remove the control knobs by easing the end caps off and undoing the collet. Release the four Allen screws under the handles which connect the front panel to the side panels, and lift the front panel away.

The power supply unit, associated printed circuit cards, mounting plate, heatsink and back panel plate are removed as one unit. Disconnect the spade terminals by loosening the connections and pushing the connector strips down. Undo the four M3.0 outside screws on the heatsink and remove the PSU assembly.

Notes:—

1. After replacing printed circuit cards make sure the nylon clamps are fully engaged.
2. Do not run the TBC for extended periods with top and bottom covers removed as the cooling flow will be impaired.

5.3 FAN FILTER

The fan filter must be cleaned regularly to ensure free ventilation of the TBC-2002.

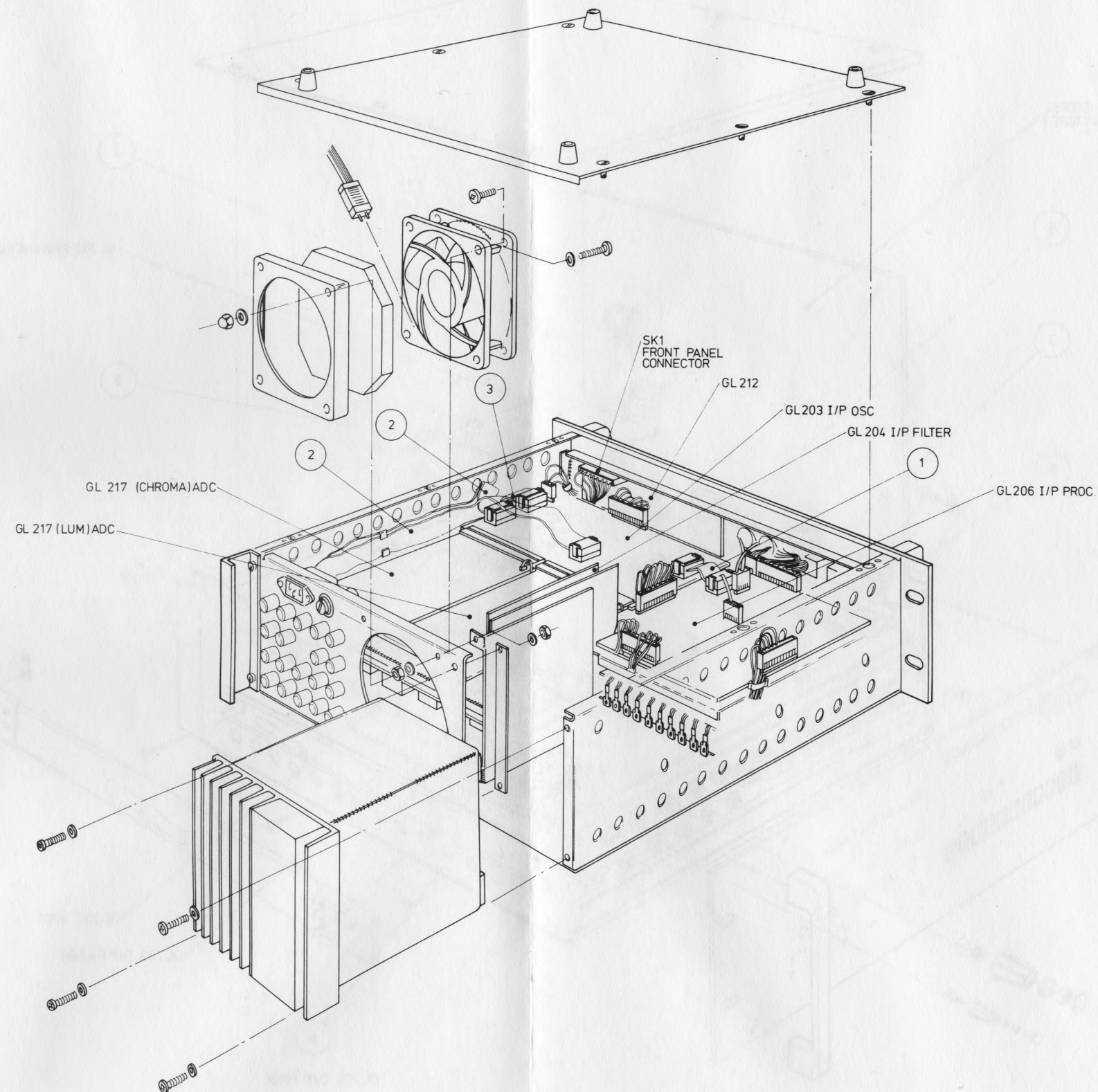


FIGURE 5.1 TBC-2002 BOTTOM VIEW

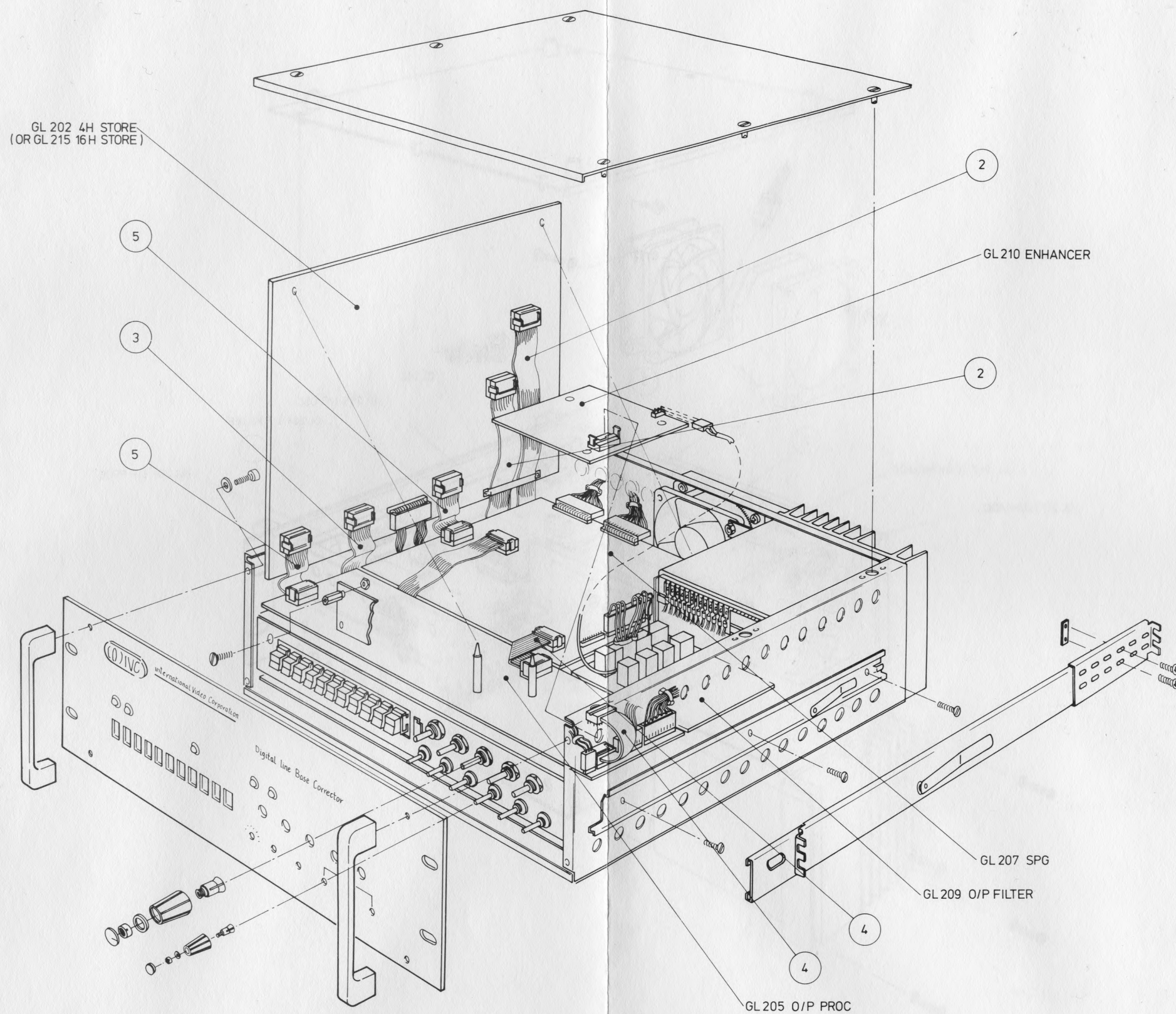


FIGURE 5.2 TBC-2002 TOP VIEW

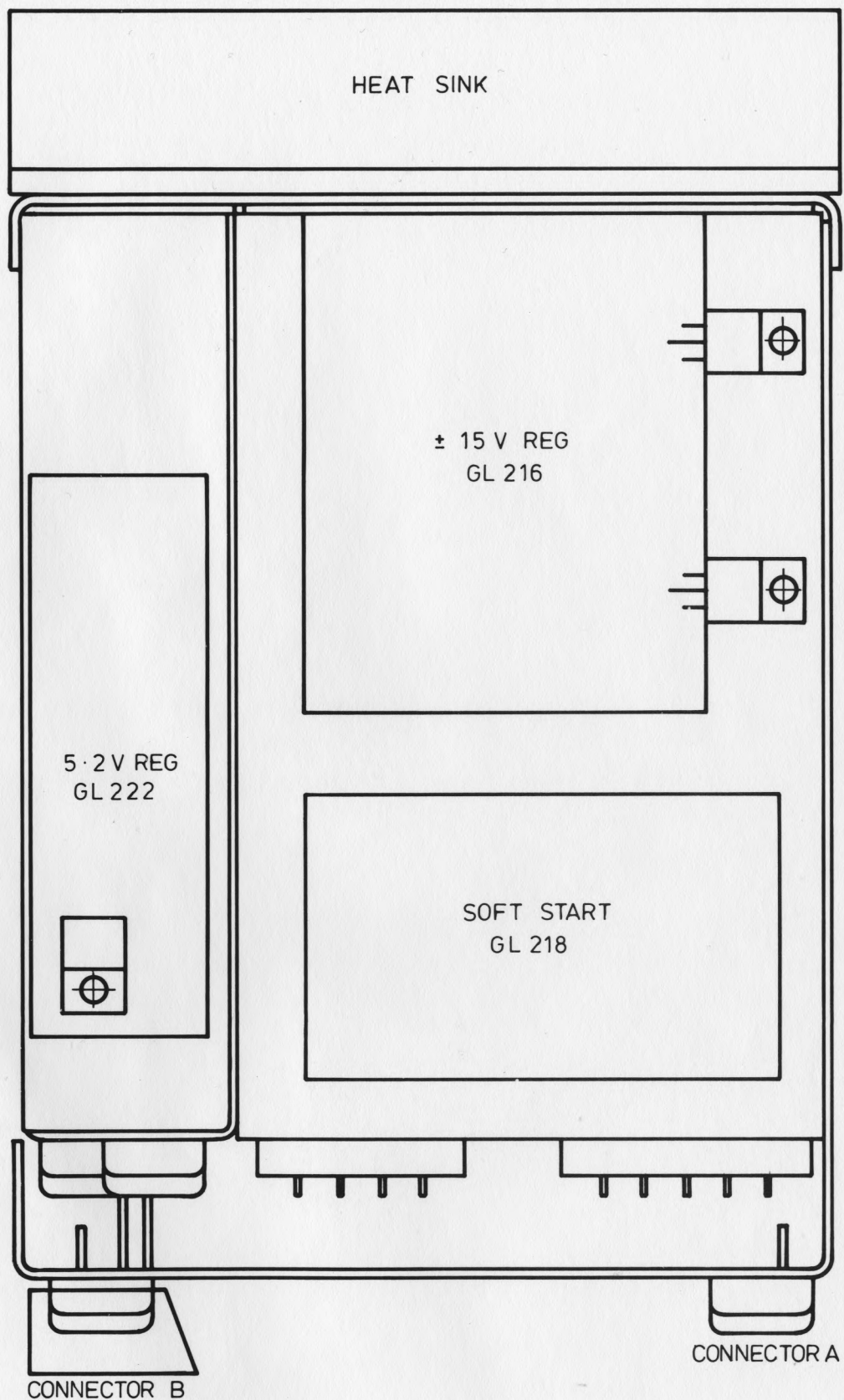


FIGURE 5.3 PSU ASSEMBLY

SECTION 6

CIRCUITS, ALIGNMENT AND PARTS LISTS

6.1 OVERALL ALIGNMENT

6.2 WIRING AND INTERCONNECTIONS

6.3 PRINTED CIRCUIT CARDS AND MODULES

Front Panel	FP
Input Processor card	GL206
Input Oscillator card	GL203
Input Filter card	GL204
ADC cards	GL217
4H Store card	GL202
16H Store card	GL215
Output Processor card	GL205
Enhancer card	GL210
Output Filter card	GL209
SPG card	GL207
Quad Dub card	GL211
Power Arrangements	POWER
Soft Start card	GL218
$\pm 15V$ Regulator card	GL216
$-5.2V$ Regulator card	GL222
Power Supply Unit	PSU

SECTION 6

CIRCUITS, ALIGNMENT AND PARTS LIST

6.1 OVERALL ALIGNMENT

Detailed circuit descriptions and alignments for each printed circuit card are included in subsection 6.3. The overall system alignment procedures are described below and involve sequential adjustments on more than one printed circuit card. The procedure below will enable alignment of a TBC-2002 returned for service after rectification of a specific fault.

6.1.1 Adjustment of Delay Line Decoder

- TP22 I/P
TP16 osc.
- a) Connect a colour bar feed to the TBC-2002 input.
 - b) On an oscilloscope with an X-Y display, monitor R-Y and B-Y outputs of decoder IC12/1 and 3 on the Input Processor card. (Note: it is not important which axis is R-Y and which is B-Y).
 - c) Adjust the delay line phase by means of cores in the 1M glass delay line until pairs of dots on the display coincide.
 - d) Using a high impedance probe connected to a vectorscope, monitor IC12/5 on the Input Processor card. Adjust the delay line amplitude balance control, RV5, for a straight line on the vector display. Note that for this measurement it is necessary to lock the vectorscope to an external feed of subcarrier which is equal in frequency to the subcarrier on the colour bar signal.
 - e) Adjust the burst gate position by means of L1 on the Input Oscillator card. Tune L1 for minimum subcarrier colour bar amplitude at the output of the TBC-2002.

6.1.2 Overall Timing Adjustments

Note that before carrying out these timing adjustments it is important to ensure that the 106MHz phase-locked loop on the SPG card and the 28.8MHz phase-locked loop on the Store card are in correct adjustment as static phase errors in these loops will affect picture and sync timing.

Monochrome Timing

- a) Select MONO and EXT video lock modes on the TBC-2002, and loop the staircase or pulse-and-bar signal through the external locking input to the main video input.
- b) On a dual trace oscilloscope, observe both the input and output signals.
- c) Adjust the front panel H timing control for coincidence of the input and output H sync pulses.
- d) Adjust RV2 on the Store card for horizontal coincidence of picture detail on the input and output signals.
- e) The TBC-2002 should now be able to be switched from BYPASS to PLAYBACK with no change in horizontal timing of the signal coming from the output connector.

Colour Mode Timing Adjustments

- a) Loop a staircase or pulse-and-bar signal with colour burst through the locking input and into the VIDEO IN input. On the ADC card, observe the input signal on TP1 on one trace and the clock signal on TP4 on the other trace.

- b) With the TBC-2002 in monochrome mode, measure the time from the leading edge of H syncs on the input signal at TP1 to the first clock pulse positive-going edge at TP4.
- c) Switch the TBC-2002 to colour mode and adjust RV7 on the Input Processor card so that the time measured in step b) is the same for monochrome and colour modes.
- d) Observe the input and output of the TBC-2002 on the two traces of the oscilloscope. Adjust RV3 on the SPG card for coincidence of luminance picture detail.
- e) Adjust RV11 on the Output Processor card for coincidence of input and output horizontal sync pulses.

6.1.3 Adjustment of Output Coder

- a) It is necessary to ensure the delay line decoder alignment (in 6.1.1) is correct before proceeding with the coder alignment.
- b) Connect a colour bar signal to the input of the TBC-2002 and observe the output on a vectorscope.
- c) Adjust RV3 (quadrature) on the Output Processor card so that the amplitude of the burst on a +V line is equal to that on a -V line, i.e. lengths of burst vectors are equal.
- d) Adjust RV7 for chroma balance during blanking time on the V axis, and RV8 on the U axis.
- e) Adjust RV8 on the chroma ADC card for V axis balance during active picture time, and RV1 on the Input Oscillator card for U axis balance.

- f) Switch off the U axis on the input colour bar source and adjust RV6 on the Output Processor card so that pairs of dots on the vector display superimpose. This is the V axis symmetry control.
- g) Switch the U axis on again and adjust RV9 for correct U to V amplitude ratio.
- h) Adjust RV4 and RV5 for correct amplitude burst with correct quadrature.

6.2 WIRING AND INTERCONNECTIONS

Each card description in sub-section 6.3 includes information on the connections to and from the card. The table below gives re-ordering information for the inter-card ribbon cables. Reference should be made to Section 5, Figures 5.1 and 5.2, for their location.

RIBBON CABLES

REF. (Fig. 5.1,5.2)	CONNECTION	PART NO.
1	GL206/SK1 – GL203/SK6	R890187
2	{ GL203/SK1 – GL202/SK6 GL203/SK2 – GL202/SK5	R891001 R891001
3	GL203/SK5 – GL202/SK4	R891055
4	{ GL205/SK2 – GL207/SK2 GL205/SK4 – GL210/SK1	R891025 R891025
5	{ GL205/SK1 – GL202/SK3 GL207/SK1 – GL202/SK1	R890035 R890035

FRONT
PANEL

FRONT PANEL

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COMPONENT SCHEDULE	1

FIGURE 1 CIRCUIT DIAGRAM, FRONT
 PANEL SWITCHES

FIGURE 2 CIRCUIT DIAGRAM, FRONT
 PANEL CONTROLS

FRONT PANEL

INTRODUCTION

The eleven potentiometer controls are hard-wired direct to the 2-part connectors mounted on the appropriate printed circuit cards. The eleven rocker switches are mounted on a printed circuit

card behind the front panel, and are hard-wired to the appropriate printed circuit cards via 2-part connector SK1.

The functions of the controls are described in detail in Section 3 of this manual.

COMPONENT SCHEDULE

CONTROL	DESCRIPTION	PART NO.
POWER ON/OFF	2-way DPDT rocker switch	R717203
COMP VIDEO/SYNCS	2-way SPDT rocker switch	R717101
REF INT/EXT	2-way SPDT rocker switch	R717101
CAPSTAN SERVO/NON C.S.	2-way SPDT rocker switch	R717101
TRACK FAST/SLOW	2-way SPDT rocker switch	R717101
QUAD DUB/NORM	2-way SPDT rocker switch	R717101
NON STD SYNC/ NORM	2-way SPDT rocker switch	R717101
PAL COLOUR/MONO	2-way SPDT rocker switch	R717101
DIRECT COLOUR/HET	2-way SPDT rocker switch	R717101
DOC ON/OFF	2-way SPDT rocker switch	R717101
PLAYBACK/BYPASS/RECORD	3-way SPDT rocker switch	R717103
VIDEO GAIN	Potentiometer, 220R	R495224
CHROMA GAIN	Potentiometer, 22k	R495226
BLACK LEVEL	Potentiometer, 1k0	R495105
V PHASE (AUTO)	Potentiometer, 22k with switch	R498226
PICTURE ENHANCE	Potentiometer, 22k with switch	R498226
CHROMA DELAY	Selector switch	R721002
SYSTEM H PHASE	Potentiometer, 22k	R495226
SYSTEM SC PHASE		
FINE	Potentiometer, 22k	R495226
COARSE	Selector switch	R721002
CHROMA PHASE	Potentiometer, 22k	R495226
VELOCITY COMP	Potentiometer, 22k	R495226

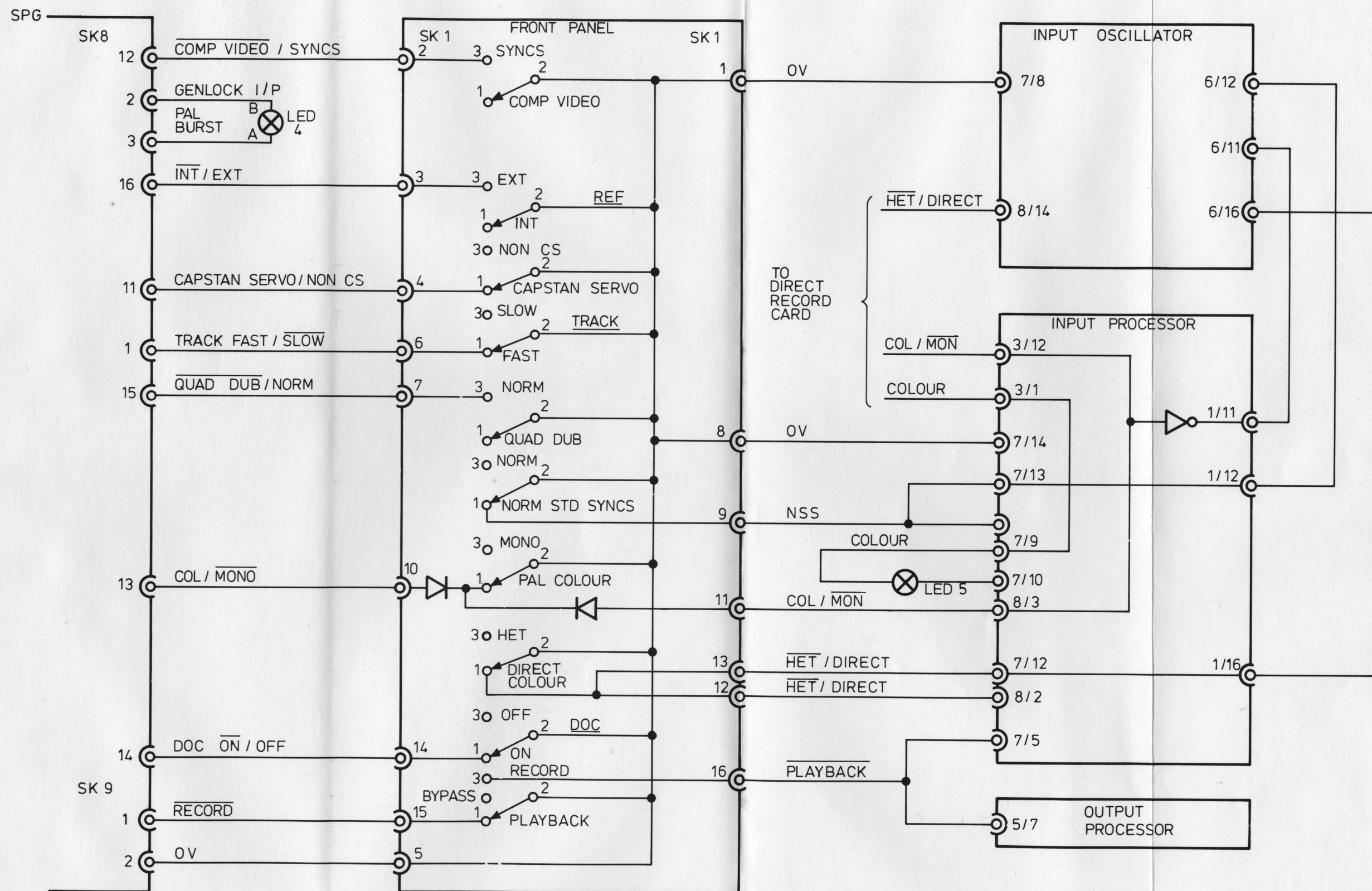


FIGURE 1 CIRCUIT DIAGRAM, FRONT PANEL SWITCHES

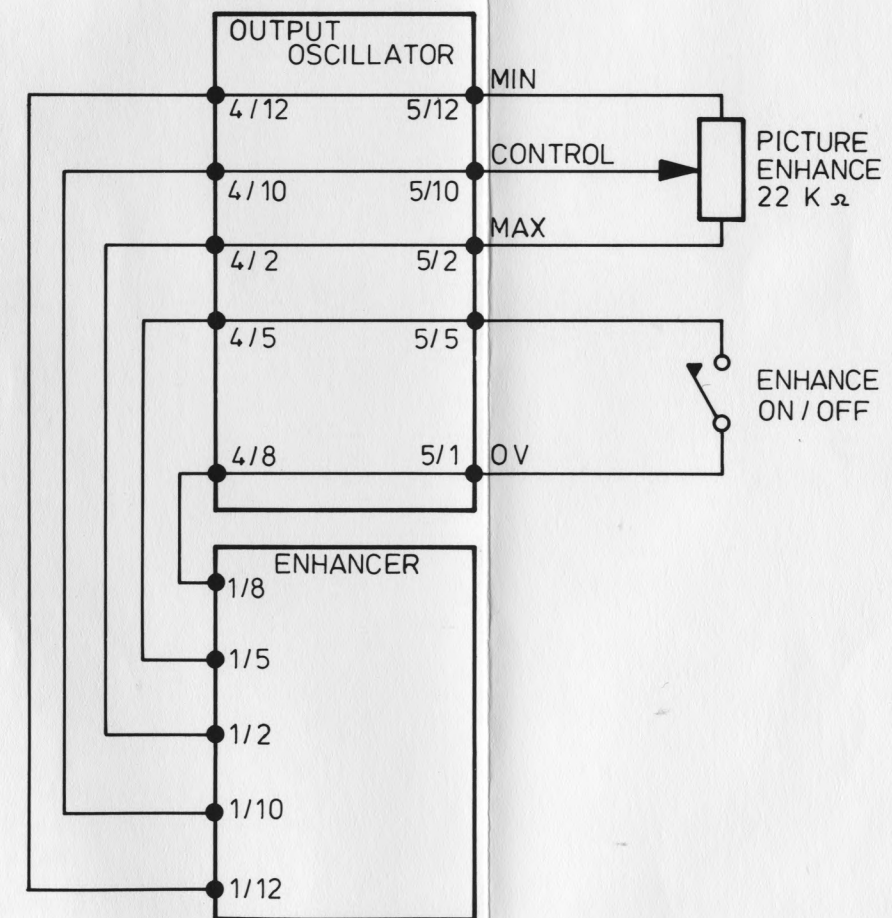
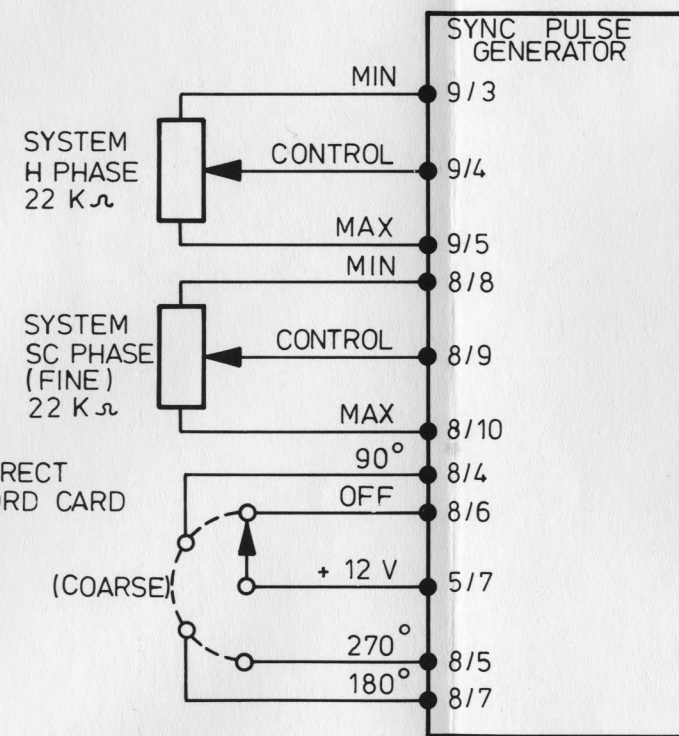
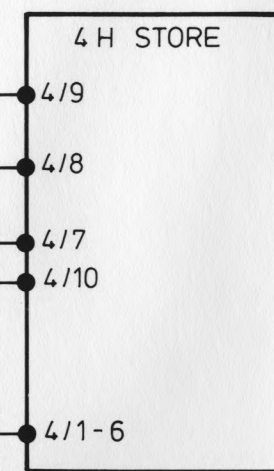
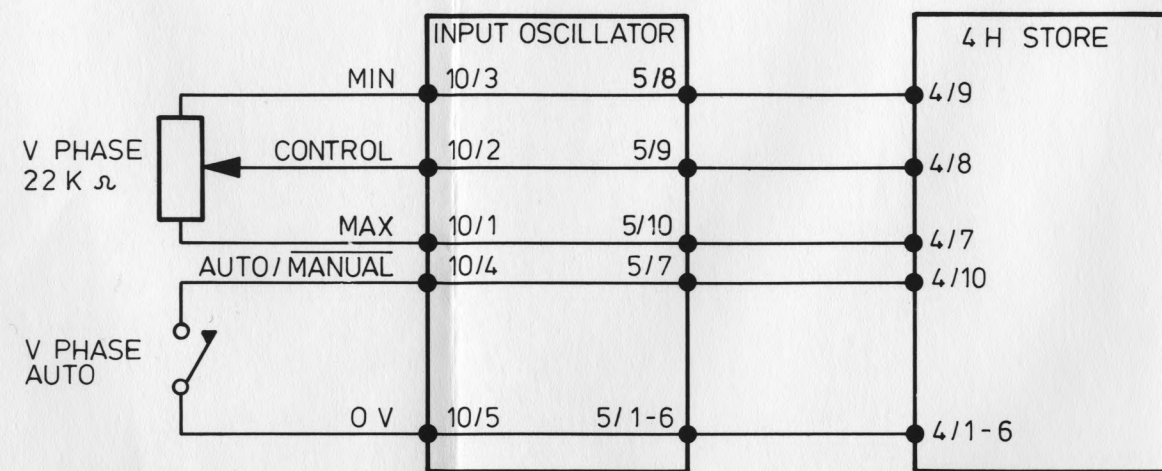
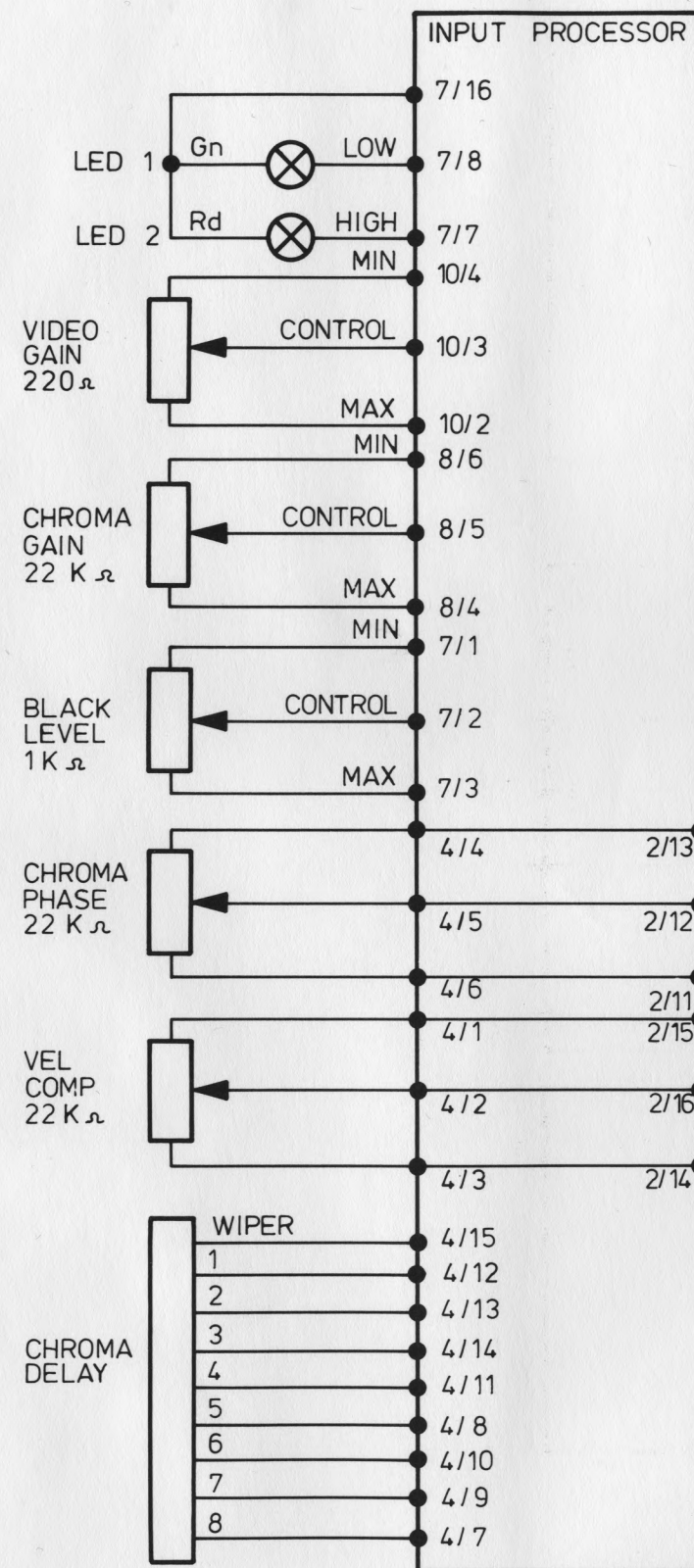


FIGURE 2 CIRCUIT DIAGRAM, FRONT PANEL CONTROLS

INPUT
PROCESSOR

INPUT PROCESSOR
IVC PCB GL206

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CIRCUIT DESCRIPTION	1
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TEST POINTS	5
COMPONENT SCHEDULE	6

FIGURE 1	BLOCK DIAGRAM
FIGURE 2	COMPONENT LAYOUT
FIGURE 3	CIRCUIT DIAGRAM

INPUT PROCESSOR

IVC PCB GL206

INTRODUCTION

The Input Processor card contains the circuits for separating the luminance and chrominance components from the incoming video signal, the sync separator circuits, and the BYPASS circuits. It also contains the chrominance demodulator and luminance/chrominance delay adjustments.

CIRCUIT DESCRIPTION

The off tape input signal VIDEO IN from the BNC connector on the rear panel enters the Input Processor card at SK5/2 and is connected into the sync separator circuit. It is connected into the clamp amplifier circuit via the BYPASS select circuit.

BYPASS Mode

The BYPASS mode is selected by the PLAYBACK/BYPASS/RECORD switch on the front panel. The TBC-2002 will, however, go into the BYPASS mode automatically in the event of a power failure within the unit.

With PLAYBACK selected on the front panel, relay RL1 is energised and its two contacts connect the incoming video signal into the first stage of the clamp amplifier circuit via the VIDEO GAIN control also on the front panel.

With BYPASS selected, the relay is de-energised and contact RL1/B connects the VIDEO IN signal direct to the Output Processor card via SK5/4. Contact RL1/A connects the video signal from the input amplifier stage of the sync separator circuit (TR29) into the clamp amplifier circuit to ensure that the TBC-2002 stays locked in "bypass" condition.

Sync Separator

The input VIDEO IN signal from the rear panel is ac coupled via C51 to the high impedance input of dual FET TR27a and b which, with TR28 and TR29, forms an amplifier with a gain of approximately 3.7. The emitter of TR29 provides two outputs. One passes via R124 to a contact of the bypass relay (RL1/A) and is used as the input to the clamp amplifier circuit in BYPASS mode. The other passes via low pass filter L4, C53, L1, C54 and is switched into the sync separator circuit via TR30. The low pass filter is Gaussian and has a cut-off frequency of 1MHz. The emitter of TR30 provides the input to the standard and non-standard sync separators.

For non-standard syncs, the emitter of TR30 is coupled to the base of TR53 via capacitor C74. TR53 dc restores the sync tips on its base emitter diode, and the separated syncs are coupled via D17 and R165 to the base of inverter TR54. D18 provides a degree of positive feedback on the leading edge of syncs. With NON STD SYNC selected on the front panel, the NSS signal at SK8/1 enables the syncs through IC4/10 to IC4/2.

For standard syncs, the emitter of TR30 is coupled via clamp capacitor C55 to the diode bridge clamp circuit D8-D11. This is driven by TR31 and TR32, and the CLAMP pulse from IC7/13 feeds the base of TR32 via R132. The video signal, with its back porch clamped to 0V, is fed to the base of TR33 whose emitter is connected through TR34 to emitter load resistor R135. TR34 is arranged to come out of saturation and clip the signal when the emitter of TR33 rises above 0.7V. The clipped video signal is applied to one input of differential comparator IC1/4, and also to the input of a peak detector circuit comprising TR35, TR36, TR37.

The peak sync voltage applied to the base of TR35 is held on C58. When TR39 is saturated, this voltage is divided by two by R141 and R147 in parallel with R148, and is applied via emitter follower TR38 to the other input of differential comparator IC1/3. This voltage is equal to half the sync pulse amplitude of the signal on IC1/4.

The separated mixed sync signal appears at TTL level at IC1/9. It is enabled through to IC4/11 by the $\overline{\text{NSS}}$ signal from IC9/10, and gated with the signal from the non-standard sync separator. The selected true and inverted mixed syncs signals are available at IC4/3 and IC5/11 respectively.

IC2 is part of an anti-latch-up circuit which measures the width of the separated sync pulses by integrating them via R155, R156, D15, C63 and comparing the resultant integrated voltage with a fixed voltage determined by R153 and R154. The integrated voltage is input to IC2/3, and the fixed voltage to IC2/2. For stable operating conditions, IC2/3 is at a lower voltage than IC2/2 so that IC2/6 is low and TR39 is saturated. If however the voltage at IC2/3 is greater than that at IC2/2, this implies that the separated sync pulse width is greater than approximately $8\mu\text{s}$ and that IC1 is slicing through picture information and not sync pulses. In this case IC2/6 goes high and switches off TR39. This sets the voltage at IC1/3 to $\frac{3}{4}$ of the peak detected voltage and ensures that IC1 is slicing through sync pulses (note that the sync to picture ratio is 3:7). Immediately sync pulses of the correct width are produced at IC1/9, IC2/6 goes low and the system continues in its stable condition.

The true mixed syncs signal from IC4/3 triggers monostable IC3/5 on the positive going edge to produce $63\mu\text{s}$ pulses at the Q and $\overline{\text{Q}}$ outputs. These pulses are set by RV8. The signal is also connected to the base of TR40 via R159. TR40 discharges C64 when the mixed syncs are high, and allows C64 to charge via R157 during sync time. The time constant, C64, R157 is so arranged that C64 only charges to the threshold of IC7/10 (approximately 1.8V) during the broad pulses of the field group. When IC7/10 crosses the threshold, the monostable is triggered and produces a 1ms true and inverted FIELD pulse at IC7/5 and 12 respectively. The FIELD pulse from IC7/5 is applied to the input clamp amplifier via D24 to inhibit the clamp pulses during the 1ms FIELD pulse; it is output to the Input Oscillator card via SK1/13, and is used to trigger monostable IC17. This is set by RV9 to output a 19.5ms pulse at pin 6 so that the cathode of D28 is pulled low and inhibits C64 from charging until the end of the pulse. This ensures that no spurious field pulses are produced by drop-outs in the input signal. The

FIELD pulse from IC7/12 disables the automatic chroma control voltage via TR56 during the field period.

The inverted mixed syncs signal from IC5/11 triggers monostables IC6/2 and IC6/10 on the positive edge (i.e. the leading edge of sync). The Q output at IC6/12 provides the horizontal blanking pulses of approximately $10\mu\text{s}$. The Q and $\overline{\text{Q}}$ outputs at IC6/13 and 4 provides the $4.5\mu\text{s}$ horizontal rate pulses (H SYNCs).

The $63\mu\text{s}$ pulse from IC3/7 inhibits the twice horizontal frequency components at IC6/1 and 9 via IC5/8 during the field group. The $63\mu\text{s}$ pulse from IC3/6 is applied to IC10/1. This NAND gate forms an R-S flip-flop with IC10/11. IC10/1 is triggered at the end of each $63\mu\text{s}$ pulse and resets IC10/11 low. IC10/11 is set high by the trailing edge of the next mixed syncs pulse from IC5/11. The positive-going edge from IC10/11 triggers monostable IC7/2 to produce CLAMP pulses at the Q and $\overline{\text{Q}}$ outputs.

The $\overline{\text{Q}}$ output from IC6/4 is taken to the Direct Record card (if used) as the H SYNC signal via SK3/13; clears monostable IC7/3 so that CLAMP pulses cannot be generated during horizontal sync time, and is applied to IC8 gate configuration. These gates are connected as a delay switch for the horizontal syncs to accommodate the difference in delay between the 5.5MHz monochrome and 3.0MHz colour low pass filters on the Input Filter card. RV7 sets the delay for the colour mode, and the H SYNCs signal is gated through by the COL/MON or MON/COL signals as appropriate and taken via SK1/10 to the Input Oscillator card as the H PULSE. The Q output from IC6/13 is coupled via C60 to the base of TR37 in the peak detector circuit.

The FLYWHEEL fH signal from the Input Oscillator card is input at SK1/9 and triggers the burst gate monostable at IC3/11 to produce BURST GATE pulses at IC3/10.

The horizontal blanking pulses and the BURST GATE pulses are combined into a three level 'sandcastle' pulse by the circuit comprising TR41, TR42, TR43. This pulse is input to the chroma demodulator circuit at IC12/15. A similar circuit consisting of TR44, TR45, TR46 combines the horizontal blanking pulses and the clamp pulse (from IC7/13) to produce a three level pulse which is input to the ACC amplifier at IC13/7.

Input Clamp Amplifier

The VIDEO IN signal from SK5/2 is switched into the input clamp amplifier circuits via the VIDEO GAIN control on the front panel. The signal from the wiper of the control is coupled to

the base of TR7 via R5. TR7 and TR8 form an emitter coupled complementary pair with TR9 as a current source. The difference voltage between the bases of the complementary emitter followers TR10 and TR11 is set by Zener diode D2. A negative feedback path is provided via R27, R30, R25, D22, R26. The amplifier provides two 75 ohm outputs at the junctions of R28, R31 and R29, R32. One output is connected to the Input Filter card via SK6/2, and the other output (monitored on TP1) provides the inputs to:

- a) the clamp comparator input filter via R33
- b) the sync amplitude indicator (VIDEO LOW) circuit via D19
- c) the chroma demodulator via R55.
- d) the Direct Record card via SK6/4.

The clamp comparator input filter is a low pass filter circuit in which CV6 resonates with L2 to provide a subcarrier frequency notch. When TR15 is turned on by a CLAMP pulse from IC7/4, the ratio of the currents flowing in TR13 and TR14 depends upon their relative base voltages. The base of TR13 is connected to the low pass filtered video signal, while the base of TR14 is connected to the black level reference voltage from the BLACK LEVEL control on the front panel via SK7/2. The collector of TR13 is connected to the base of TR17, while the collector of TR14 is connected to the base of phase inverter TR16. Thus opposing currents via TR17 and TR18 charge or discharge C18 via R52 during the CLAMP pulse period depending on whether the video signal voltage is lower or higher than the reference voltage. At the end of the CLAMP pulse, TR15 is turned off, the emitters of TR13 and TR14 are held positive with respect to their base potentials by the combination of R37, R209, and TR17, TR18 are also turned off. The potential on C18 is therefore held for the duration of the next line. The voltage on C18 controls the current of TR1 which is opposed by fixed current source TR2. The difference between the two currents charges or discharges the input coupling capacitor C1. During the vertical interval, the CLAMP pulses and TR1 and TR2 are inhibited by the FIELD pulse applied to the bases of TR3 and TR4 via R16.

For NON STD SYNC mode, the input signal is ac coupled via C1 to the input of the clamp amplifier, and the BLACK LEVEL control on the front panel adjusts the mean dc level of the signal. This ac coupling is a good compromise for signals input from the simple monochrome cameras which use mean level target voltage control. In this mode the clamp circuitry is disabled in a similar way as described for normal sync operation. TR5 is turned

on by the NSS signal from IC9/10 and turns on TR4. At the same time TR6 is turned off and turns FET TR19 on. This connects the potential at the junction of R42 and the cathode of D23 through R11, R5 to the base of TR7. The base of TR20 is connected through R210 to the wiper of the BLACK LEVEL control. Adjustment of this control will therefore determine the dc voltage at the output of the clamp amplifier.

The state of the input signal is indicated by two LEDs on the front panel above the VIDEO GAIN control. These LEDs are controlled by comparators IC11, one of which looks at the voltage level, and the other at the sync level. The peak positive voltage after the low pass filter at the junction of L2 and C11 is held by D20, C49. This voltage, which is at IC11/8, is compared against a reference at IC11/9 set by RV2. When IC11/8 is greater than IC11/9, IC11/4 goes low and lights up the red LED to indicate that the input signal level is too high. Similarly, the peak sync pulse level at TP1 is held by D19, C50 (IC11/11) and compared against a voltage set by RV3 (IC11/10). If the voltage at IC11/11 is more negative than that at IC11/10 the green LED lights up to indicate that the sync level is adequate. TR22 compensates for black level changes.

Chroma Demodulator Circuits

The chroma components of the signal from the input clamp amplifier (monitored by TP1) are coupled through R55 and transformer T1 to the balanced inputs of IC13 (pins 1 and 2). The output at IC13/6 is coupled to the delay lines DL2 and DL3 via amplifier TR23. Each tap of the delay lines is connected to the input of a transmission gate IC14, IC15, and the outputs of the transmission gates are connected in parallel. Only one transmission gate at a time may be turned on by the CHROMA DELAY front panel switch via SK4.

The output of the selected transmission gate is connected to the base of TR24 whose collector is connected to the 1H glass delay line DL1. The outputs of DL1 are input to the demodulator IC12/5 and 6 via position A (DELAY LINE PAL) of switch SW1. The undelayed signal at the emitter of TR24 is attenuated by RV5 the wiper of which is connected to the centre tap of the output transformer of DL1 (pin 4). RV5 is adjusted to give correct delay line amplitude balance.

The colour difference signal R-Y is output at IC12/3, and B-Y is output at IC12/1. These signals are taken to the Input Oscillator card via SK1/14 and 15 respectively.

The demodulator looks at the burst amplitude of the chroma signal during the burst gate period

as indicated by the three level 'sandcastle' pulse at IC12/15. If the amplitude of the burst is at the wrong level IC12 feeds back ACC voltage to IC13 via TR56 and LK1 to automatically correct the chroma amplitude. The TEST position of LK1 allows a fixed voltage to be applied to IC13/3 for non-automatic chroma control. This voltage is adjusted by RV6.

The output from IC12/16 is the colour kill signal which is input to comparator IC11/7. It is compared against the input at IC11/6 which is derived from RV4 for colour operation and from TR25 for monochrome operation. For colour operation, the output at IC11/1 is used as the COLOUR control for the Output Processor card (via SK7/11) and for the LED on the front panel (via SK7/9). For monochrome operation, TR25 is turned on by the COL/MON signal at SK8/3 via IC10/4 and ensures the colour kill facility is enabled. The facility may be disabled by LK2.

ADJUSTMENTS

CV3 — Adjusts the free running frequency of oscillator X1. Disconnect the video input to the TBC-2002 and trigger an oscilloscope with a local stable subcarrier frequency on one trace. Observe IC12/10 on the other trace, and adjust CV3 for zero beat (8.8MHz squarewave on IC12/10).

CV4,— Adjust twitter on the PAL delay line into CV5 the demodulator IC13. These are accurately set at the factory and should not be adjusted on site.

CV6 — Adjusts subcarrier frequency. This is factory set, and no attempt should be made to readjust on site.

RV2 — Adjusts the threshold level of the red VIDEO HIGH LED (peak white) on the front panel.

RV3 — Adjusts the threshold level of the green VIDEO LOW LED (sync amplitude) on the front panel.

RV4 — Adjusts the threshold of the green PAL COLOUR LED on the front panel.

RV5 — Adjusts the balance of the chroma delay line. See section on adjustment on decoder.

RV6 — Adjusts the chrominance level in non automatic chroma control. (Test position only)

RV7 — Adjusts the timing of the write clock pulses (H PULSE) between monochrome and colour mode.

RV8 — Sets the period of the 'half line remover' monostable IC3/7. Adjust for a high pulse period of 1μs at IC3/7.

RV9 — Sets the field lockout period. It is adjusted to give a pulse width of 19.5ms at IC17/6.

LK1 — Selects automatic chroma control when in position B-C, and non automatic control in position A-B. Position A-B is generally used for test purposes.

LK2 — Selects colour kill operation. Inhibits colour kill mode in position A-B; selects normal colour kill in position B-C.

CONNECTIONS

SK1 Input Oscillator card connections.

1,2,3,4	Ground
8	CLAMP pulse
9	FLYWHEEL fH
10	H PULSE
11	MON/COL
12	NSS
13	FIELD pulse
14	Colour difference R-Y
15	Colour difference B-Y
16	HET/DIRECT

SK2 Direct card connections

1	Chroma delay 8
2	Chroma delay 5
3	Chroma delay 7
4	Chroma delay 6
5	Chroma delay 4
6	Chroma delay 1
7	Chroma delay 2
8	Chroma delay 3
9	+12V, chroma delay control
10	Chroma delay 4
11 } 12 } 13 }	Chroma phase control
14 } 15 } 16 }	Vel comp control

SK3	Direct card connections	SK7	Front Panel Switches
1	COLOUR	1	Minimum, BLACK LEVEL control
2	+12V	2	BLACK LEVEL control
4	-15V	3	Maximum, BLACK LEVEL control
5	-5V	5	PLAYBACK
6	+15V	6	Earth, Video gain LEDs
7	+5V	7	VIDEO HIGH
8	+12V switched	8	VIDEO LOW
9,10	Ground	9	COLOUR (to LED)
11	FIELD pulse	11	COLOUR (to O/P Proc)
12	COL/MON	12	HET/DIRECT
13	H SYNC	13	NSS
14	CHROMA GAIN control		
15	H PULSE	SK8	Control connections
16	MON/COL	1	NSS
SK4	Connections from Front Panel Controls	2	HET/DIRECT
1 } 2 } 3 }	VEL COMP control	3	COL/MON
4 } 5 } 6 }	CHROMA PHASE control	4	Maximum, CHROMA GAIN
7	Chroma delay 8	5	CHROMA GAIN control
8	Chroma delay 5	6	Minimum, CHROMA GAIN
9	Chroma delay 7	7	MONO + NSS
19	Chroma delay 6	8	+5V
11	Chroma delay 4	SK9	Power connections
12	Chroma delay 1	2	+15V
13	Chroma delay 2	3	0V
14	Chroma delay 3	4,5,6	+5V
15	+12V, chroma delay control	7,8,10	0V
SK5	Video connections (input and bypass)	11,12	-5.2V
1	Ground, VIDEO IN	13,14	0V
2	VIDEO IN	15	-15V
4	BYPASS	SK10	Video Gain Control connections
5	Ground, BYPASS	2	Maximum, VIDEO GAIN
SK6	Video connections (Input Filter and Direct Record cards)	3	VIDEO GAIN control
1	Ground, LUM	4	Minimum, VIDEO GAIN
2	LUM		
4	VIDEO	TEST POINTS	
5	Ground, VIDEO	TP1	Luminance signal from clamp amplifier
		TPG	Ground

CIRCUIT REF.	DESCRIPTION	PART NO.
	CAPACITORS	
C1	1 μ F $\pm$ 10%, 63V	R521055
C2	Not fitted	—
C3 – C6	1 μ F $\pm$ 10%, 63V	R521055
C7	10nF, 25V	R501033
C8	47pF $\pm$ 5%, 63V	R514705
C10	22pF $\pm$ 5%, 63V	R512205
C11	330pF $\pm$ 5%, 63V	R513315
C12	Not fitted	—
C13	Not fitted	—
C14	100pF $\pm$ 5%, 63V	R511015
C15	470nF $\pm$ 10%, 63V	R524745
C16	100nF $\pm$ 10%, 100V	R521046
C17	47pF $\pm$ 5%, 63V	R514705
C18	220nF $\pm$ 10%, 63V	R522245
C19	470nF, 16V	R544742
C20	1 μ F, 35V	R541052
C21	Not fitted	—
C22	Not fitted	—
C23	22 μ F, 16V	R542262
C24	10nF, 25V	R501033
C26	10nF, 25V	R501033
C28	10nF, 25V	R501033
C29	22pF, 63V	R512205
C31	220nF $\pm$ 10%, 63V	R522245
C32	1 μ F, 35V	R541054
C33	22nF $\pm$ 10%, 100V	R522236
C34	1 μ F, 35V	R541054
C35	100nF $\pm$ 10%, 100V	R521046
C37	47 μ F, 16V	R544762
C38	10nF, 25V	R501033
C39 – C46	Not fitted	—
C47	10nF, 25V	R501033
C48	10nF, 25V	R501033
C49	100nF $\pm$ 10%, 100V	R521046

CIRCUIT REF.	DESCRIPTION	PART NO.
	CAPACITORS (continued)	
C50	100nF $\pm 10\%$, 100V	R521046
C51	100nF $\pm 10\%$, 100V	R521046
C52	Not fitted	—
C53	150pF, 63V	R511515
C54	470pF, 63V	R514715
C55	220nF $\pm 10\%$, 63V	R522245
C56	47nF $\pm 10\%$, 100V	R524736
C57	47nF $\pm 10\%$, 100V	R524736
C58	470nF $\pm 10\%$, 63V	R524745
C59	47pF, 63V	R514705
C60	220pF, 63V	R512215
C61	10nF, 25V	R501033
C62	10nF, 25V	R501033
C63	22 μ F, 63V	R542265
C64	10nF $\pm 10\%$, 100V	R521036
C65	220pF, 63V	R512215
C66	56pF, 63V	R515605
C67	100nF $\pm 10\%$, 100V	R521046
C68	220pF, 63V	R512215
C69	820pF, 63V	R518215
C70	100pF, 63V	R511015
C71	220pF, 63V	R512215
C72	Not fitted	—
C73	220pF, 63V	R512215
C74	22nF $\pm 10\%$, 100V	R522236
C75	100pF, 63V	R511015
C76	10nF, 25V	R501033
C77	Not fitted	—
C78	100nF $\pm 10\%$, 100V	R521046
C79	1nF, 63V	R511025
C80	10 μ F, 35V	R541064
C81	22 μ F, 6.3V	R542261
C82	22 μ F, 6.3V	R542261
C83	10 μ F, 35V	R541064

CIRCUIT REF.	DESCRIPTION	PART NO.
	CAPACITORS (continued)	
C84 – C100	10nF, 25V	R501033
C101	47 μ F, 16V	R544762
C102	47 μ F, 16V	R544762
C103	10nF, 25V	R501033
C104	10nF, 25V	R501033
C105	220nF $\pm$ 10%, 63V	R522245
CV1, CV2	Not fitted	—
CV3 – CV6	2 – 22pF, variable	R591222
	DIODES	
D1	BZY88C6V8	R372088
D2	BZY88C6V8	R372088
D3	1N4148	R354148
D4	1N916	R350916
D5	1N916	R350916
D6	OA47	R385047
D7	OA47	R385047
D8	1N916	R350916
D9	1N916	R350916
D10	1N916	R350916
D11	1N916	R350916
D12	1N4148	R354148
D13	1N4148	R354148
D14	1N4148	R354148
D15	1N4148	R354148
D16	OA47	R385047
D17	1N4148	R354148
D18	1N4148	R354148
D19	1N4148	R354148
D20	1N4148	R354148
D21	BZY88C6V8	R372088
D22	BZY88C5V1	R372288
D23	1N4148	R354148
D24	1N4148	R354148
D25	1N4002	R354002

CIRCUIT REF.	DESCRIPTION	PART NO.
	DIODES (continued)	
D26	1N916	R350916
D27	BZY88C6V2	R372188
D28	1N4148	R354148
	DELAY LINES	
DL1	SDL 445	R680445
DL2	BAL 0408-A2	R680408
DL3	BAL 0408-A2	R680408
	INTEGRATED CIRCUITS	
IC1	NE529	R280529
IC2	741CN-8	R280741
IC3	14538B	R262538
IC4	4011B	R261011
IC5	74LS00	R240000
IC6	74LS221	R240221
IC7	74LS221	R240221
IC8	4011B	R261011
IC9	4001B	R261001
IC10	4011B	R261011
IC11	LM339	R280339
IC12	TDA 2522	R282522
IC13	TDA 2560	R282560
IC14	4066B	R261066
IC15	4066B	R261066
IC17	74LS122	R240122
	INDUCTORS	
L1	68 μ H	R620683
L2	33MH	R620339
L3	Not fitted	—
	RELAY	
RL1	2-pole, 6V coil	R790062
	RESISTORS	
R1	100 $\pm$ 2%, $\frac{1}{4}$ W	R445104
R2	1k2 $\pm$ 2%, $\frac{1}{4}$ W	R445125
R3	220 $\pm$ 2%, $\frac{1}{4}$ W	R445224

CIRCUIT REF.	DESCRIPTION	PART NO.
	RESISTORS (continued)	
R4	1k0 $\pm 5\%$, $\frac{1}{4}$ W	R405105
R5	330 $\pm 5\%$, $\frac{1}{4}$ W	R405334
R6	1M0 $\pm 10\%$, $\frac{1}{4}$ W	R405108
R7	15k $\pm 5\%$, $\frac{1}{4}$ W	R405156
R8	1k2 $\pm 5\%$, $\frac{1}{4}$ W	R405125
R9	270 $\pm 5\%$, $\frac{1}{4}$ W	R405274
R10	470 $\pm 5\%$, $\frac{1}{4}$ W	R405474
R11	47k $\pm 5\%$, $\frac{1}{4}$ W	R405476
R12	47k $\pm 5\%$, $\frac{1}{4}$ W	R405476
R13	100k $\pm 5\%$, $\frac{1}{4}$ W	R405107
R14	22k $\pm 5\%$, $\frac{1}{4}$ W	R405226
R15	33k $\pm 5\%$, $\frac{1}{4}$ W	R405336
R16	3k3 $\pm 5\%$, $\frac{1}{4}$ W	R405335
R17	33k $\pm 5\%$, $\frac{1}{4}$ W	R405336
R18	22k $\pm 5\%$, $\frac{1}{4}$ W	R405226
R19	4k7 $\pm 5\%$, $\frac{1}{4}$ W	R405475
R20	10k $\pm 5\%$, $\frac{1}{4}$ W	R405106
R21	4k7 $\pm 5\%$, $\frac{1}{4}$ W	R405475
R22	560 $\pm 5\%$, $\frac{1}{4}$ W	R405564
R23	33R $\pm 5\%$, $\frac{1}{4}$ W	R405333
R24	33R $\pm 5\%$, $\frac{1}{4}$ W	R405333
R25	180 $\pm 5\%$, $\frac{1}{4}$ W	R405184
R26	2k2 $\pm 5\%$, $\frac{1}{4}$ W	R405225
R27	820 $\pm 5\%$, $\frac{1}{4}$ W	R405824
R28	150 $\pm 5\%$, $\frac{1}{4}$ W	R405154
R29	150 $\pm 5\%$, $\frac{1}{4}$ W	R405154
R30	820 $\pm 5\%$, $\frac{1}{4}$ W	R405824
R31	150 $\pm 5\%$, $\frac{1}{4}$ W	R405154
R32	150 $\pm 5\%$, $\frac{1}{4}$ W	R405154
R33	270 $\pm 5\%$, $\frac{1}{4}$ W	R405274
R34	2k2 $\pm 5\%$, $\frac{1}{4}$ W	R405225
R35	1k2 $\pm 5\%$, $\frac{1}{4}$ W	R405125
R36	1k2 $\pm 5\%$, $\frac{1}{4}$ W	R405125
R37	27k $\pm 5\%$, $\frac{1}{4}$ W	R405276

CIRCUIT REF.	DESCRIPTION	PART NO.
	RESISTORS (continued)	
R38	220 $\pm 5\%$, $\frac{1}{4}$ W	R405224
R39	270k $\pm 5\%$, $\frac{1}{4}$ W	R405277
R40	8k2 $\pm 5\%$, $\frac{1}{4}$ W	R405825
R41	6k8 $\pm 5\%$, $\frac{1}{4}$ W	R405685
R42	10k $\pm 5\%$, $\frac{1}{4}$ W	R405106
R43	27k $\pm 5\%$, $\frac{1}{4}$ W	R405276
R44	22k $\pm 5\%$, $\frac{1}{4}$ W	R405226
R45	1k2 $\pm 5\%$, $\frac{1}{4}$ W	R405125
R46	2k2 $\pm 5\%$, $\frac{1}{4}$ W	R405225
R47	33k $\pm 5\%$, $\frac{1}{4}$ W	R405336
R48	1k2 $\pm 5\%$, $\frac{1}{4}$ W	R405125
R49	1k2 $\pm 5\%$, $\frac{1}{4}$ W	R405125
R50	470 $\pm 5\%$, $\frac{1}{4}$ W	R405474
R51	470 $\pm 5\%$, $\frac{1}{4}$ W	R405474
R52	15R $\pm 5\%$, $\frac{1}{4}$ W	R405153
R53	1k0 $\pm 5\%$, $\frac{1}{4}$ W	R405105
R54	1k0 $\pm 5\%$, $\frac{1}{4}$ W	R405105
R55	10k $\pm 5\%$, $\frac{1}{4}$ W	R405106
R56	4k7 $\pm 5\%$, $\frac{1}{4}$ W	R405475
R57	47k $\pm 5\%$, $\frac{1}{4}$ W	R405476
R58	10k $\pm 5\%$, $\frac{1}{4}$ W	R405106
R59	5k6 $\pm 5\%$, $\frac{1}{4}$ W	R405565
R60	2k2 $\pm 5\%$, $\frac{1}{4}$ W	R405225
R61	56k $\pm 5\%$, $\frac{1}{4}$ W	R405105
R62	1k0 $\pm 5\%$, $\frac{1}{4}$ W	R405105
R63	10k $\pm 5\%$, $\frac{1}{4}$ W	R405106
R64	12k $\pm 5\%$, $\frac{1}{4}$ W	R405126
R65	3k9 $\pm 5\%$, $\frac{1}{4}$ W	R405395
R66	10k $\pm 5\%$, $\frac{1}{4}$ W	R405106
R67	2k2 $\pm 5\%$, $\frac{1}{4}$ W	R405225
R68	1k8 $\pm 5\%$, $\frac{1}{4}$ W	R405185
R69	680 $\pm 5\%$, $\frac{1}{4}$ W	R405684
R70	Not fitted	—
R71	27k $\pm 5\%$, $\frac{1}{4}$ W	R405276

CIRCUIT REF.	DESCRIPTION	PART NO.
	RESISTORS (continued)	
R72	100 $\pm$ 5%, $\frac{1}{4}$ W	R405104
R73	180 $\pm$ 5%, $\frac{1}{4}$ W	R405184
R74	Not fitted	—
R75	10k $\pm$ 5%, $\frac{1}{4}$ W	R405106
R76 — R83	Resistor pack RP1/RP2	R478107
R84	100 $\pm$ 5%, $\frac{1}{4}$ W	R405104
R85	100 $\pm$ 5%, $\frac{1}{4}$ W	R405104
R86	560 $\pm$ 5%, $\frac{1}{4}$ W	R405564
R87	Wire link	—
R88	27k $\pm$ 5%, $\frac{1}{4}$ W	R405276
R89	1k0 $\pm$ 5%, $\frac{1}{4}$ W	R405105
R90	390 $\pm$ 5%, $\frac{1}{4}$ W	R405394
R91	10k $\pm$ 5%, $\frac{1}{4}$ W	R405106
R92	220 $\pm$ 5%, $\frac{1}{4}$ W	R405224
R93	6k8 $\pm$ 5%, $\frac{1}{4}$ W	R405685
R94	100 $\pm$ 5%, $\frac{1}{4}$ W	R405104
R95	4k7 $\pm$ 5%, $\frac{1}{4}$ W	R405475
R96	4k7 $\pm$ 5%, $\frac{1}{4}$ W	R405475
R97	10k $\pm$ 5%, $\frac{1}{4}$ W	R405106
R98	15k $\pm$ 5%, $\frac{1}{4}$ W	R405156
R99	10k $\pm$ 5%, $\frac{1}{4}$ W	R405106
R100	330 $\pm$ 5%, $\frac{1}{4}$ W	R405334
R101	4M7 $\pm$ 10%, $\frac{1}{4}$ W	R405478
R102	4M7 $\pm$ 10%, $\frac{1}{4}$ W	R405478
R103	22k $\pm$ 5%, $\frac{1}{4}$ W	R405226
R104	5k6 $\pm$ 5%, $\frac{1}{4}$ W	R405565
R105	4k7 $\pm$ 5%, $\frac{1}{4}$ W	R405475
R106	33k $\pm$ 5%, $\frac{1}{4}$ W	R405336
R107	4k7 $\pm$ 5%, $\frac{1}{4}$ W	R405475
R108	27k $\pm$ 5%, $\frac{1}{4}$ W	R405276
R109	270 $\pm$ 5%, $\frac{1}{4}$ W	R405274
R110	330 $\pm$ 5%, $\frac{1}{4}$ W	R405334
R111	4M7 $\pm$ 10%, $\frac{1}{4}$ W	R405478
R112	220 $\pm$ 5%, $\frac{1}{4}$ W	R405224

CIRCUIT REF.	DESCRIPTION	PART NO.
	RESISTORS (continued)	
R113	220 $\pm$ 5%, $\frac{1}{4}$ W	R405224
R114	1k0 $\pm$ 5%, $\frac{1}{4}$ W	R405105
R115	6k8 $\pm$ 5%, $\frac{1}{4}$ W	R405685
R116	8k2 $\pm$ 5%, $\frac{1}{4}$ W	R405825
R117	270 $\pm$ 5%, $\frac{1}{4}$ W	R405274
R118	100 $\pm$ 5%, $\frac{1}{4}$ W	R405104
R119	Not fitted	—
R120	4k7 $\pm$ 5%, $\frac{1}{4}$ W	R405475
R121	100 $\pm$ 5%, $\frac{1}{4}$ W	R405104
R122	270 $\pm$ 5%, $\frac{1}{4}$ W	R405274
R123	470 $\pm$ 5%, $\frac{1}{4}$ W	R405474
R124	220 $\pm$ 5%, $\frac{1}{4}$ W	R405224
R125	220 $\pm$ 5%, $\frac{1}{4}$ W	R405224
R126	1k0 $\pm$ 5%, $\frac{1}{4}$ W	R405105
R127	1M0 $\pm$ 10%, $\frac{1}{4}$ W	R405108
R128	150k $\pm$ 5%, $\frac{1}{4}$ W	R405157
R129	2k7 $\pm$ 5%, $\frac{1}{4}$ W	R405275
R130	2k7 $\pm$ 5%, $\frac{1}{4}$ W	R405275
R131	27k $\pm$ 5%, $\frac{1}{4}$ W	R405276
R132	4k7 $\pm$ 5%, $\frac{1}{4}$ W	R405475
R133	220 $\pm$ 5%, $\frac{1}{4}$ W	R405224
R134	100k $\pm$ 5%, $\frac{1}{4}$ W	R405107
R135	3k3 $\pm$ 5%, $\frac{1}{4}$ W	R405335
R136	220 $\pm$ 5%, $\frac{1}{4}$ W	R405224
R137	100 $\pm$ 5%, $\frac{1}{4}$ W	R405104
R138	47k $\pm$ 5%, $\frac{1}{4}$ W	R405476
R139	680 $\pm$ 5%, $\frac{1}{4}$ W	R405684
R140	680 $\pm$ 5%, $\frac{1}{4}$ W	R405684
R141	15k $\pm$ 5%, $\frac{1}{4}$ W	R405156
R142	4k7 $\pm$ 5%, $\frac{1}{4}$ W	R405475
R143	1k0 $\pm$ 5%, $\frac{1}{4}$ W	R405105
R144	100k $\pm$ 5%, $\frac{1}{4}$ W	R405107
R145	220 $\pm$ 5%, $\frac{1}{4}$ W	R405224
R146	10k $\pm$ 5%, $\frac{1}{4}$ W	R405106

CIRCUIT REF.	DESCRIPTION	PART NO.
	RESISTORS	
R147	47k $\pm 5\%$, $\frac{1}{4}$ W	R405476
R148	22k $\pm 5\%$, $\frac{1}{4}$ W	R405226
R149	100k $\pm 5\%$, $\frac{1}{4}$ W	R405107
R150	1k0 $\pm 5\%$, $\frac{1}{4}$ W	R405105
R151	1k0 $\pm 5\%$, $\frac{1}{4}$ W	R405105
R152	4k7 $\pm 5\%$, $\frac{1}{4}$ W	R405475
R153	47k $\pm 5\%$, $\frac{1}{4}$ W	R405476
R154	10k $\pm 5\%$, $\frac{1}{4}$ W	R405106
R155	10k $\pm 5\%$, $\frac{1}{4}$ W	R405106
R156	82k $\pm 5\%$, $\frac{1}{4}$ W	R405826
R157	10k $\pm 5\%$, $\frac{1}{4}$ W	R405106
R158	15k $\pm 5\%$, $\frac{1}{4}$ W	R405156
R159	10k $\pm 5\%$, $\frac{1}{4}$ W	R405106
R160	1M0 $\pm 10\%$, $\frac{1}{4}$ W	R405108
R161	220 $\pm 5\%$, $\frac{1}{4}$ W	R405224
R162	27k $\pm 5\%$, $\frac{1}{4}$ W	R405276
R163	1k5 $\pm 5\%$, $\frac{1}{4}$ W	R405155
R164	1k0 $\pm 5\%$, $\frac{1}{4}$ W	R405105
R165	2k2 $\pm 5\%$, $\frac{1}{4}$ W	R405225
R166	3k9 $\pm 5\%$, $\frac{1}{4}$ W	R405395
R167	4k7 $\pm 5\%$, $\frac{1}{4}$ W	R405475
R168	220k $\pm 5\%$, $\frac{1}{4}$ W	R405227
R169	12k $\pm 5\%$, $\frac{1}{4}$ W	R405126
R170	15k $\pm 5\%$, $\frac{1}{4}$ W	R405156
R171	18k $\pm 5\%$, $\frac{1}{4}$ W	R405186
R172	15k $\pm 5\%$, $\frac{1}{4}$ W	R405156
R173	6k8 $\pm 5\%$, $\frac{1}{4}$ W	R405685
R174	4k7 $\pm 5\%$, $\frac{1}{4}$ W	R405475
R175	47k $\pm 5\%$, $\frac{1}{4}$ W	R405476
R176	47k $\pm 5\%$, $\frac{1}{4}$ W	R405476
R177	22k $\pm 5\%$, $\frac{1}{4}$ W	R405226
R178	10k $\pm 5\%$, $\frac{1}{4}$ W	R405106
R179	10k $\pm 5\%$, $\frac{1}{4}$ W	R405106
R180	10k $\pm 5\%$, $\frac{1}{4}$ W	R405106

CIRCUIT REF.	DESCRIPTION	PART NO.
	RESISTORS (continued)	
R181	3k3 $\pm 5\%$, $\frac{1}{4}W$	R405335
R182	470 $\pm 5\%$, $\frac{1}{4}W$	R405474
R183	10k $\pm 5\%$, $\frac{1}{4}W$	R405106
R184	10k $\pm 5\%$, $\frac{1}{4}W$	R405106
R185	10k $\pm 5\%$, $\frac{1}{4}W$	R405106
R186	5k6 $\pm 5\%$, $\frac{1}{4}W$	R405565
R187	10k $\pm 5\%$, $\frac{1}{4}W$	R405106
R188	10k $\pm 5\%$, $\frac{1}{4}W$	R405106
R189	10k $\pm 5\%$, $\frac{1}{4}W$	R405106
R190	3k3 $\pm 5\%$, $\frac{1}{4}W$	R405335
R191	470 $\pm 5\%$, $\frac{1}{4}W$	R405474
R192	10k $\pm 5\%$, $\frac{1}{4}W$	R405106
R193	10k $\pm 5\%$, $\frac{1}{4}W$	R405106
R194	10k $\pm 5\%$, $\frac{1}{4}W$	R405106
R195	5k6 $\pm 5\%$, $\frac{1}{4}W$	R405565
R196	1k0 $\pm 5\%$, $\frac{1}{4}W$	R405105
R197	22k $\pm 5\%$, $\frac{1}{4}W$	R405226
R198	22k $\pm 5\%$, $\frac{1}{4}W$	R405226
R199	Not fitted	—
R200	Not fitted	—
R201	1k0 $\pm 5\%$, $\frac{1}{4}W$	R405105
R202	1k0 $\pm 5\%$, $\frac{1}{4}W$	R405105
R203	10k $\pm 5\%$, $\frac{1}{4}W$	R405106
R204	10k $\pm 5\%$, $\frac{1}{4}W$	R405106
R205	1k0 $\pm 5\%$, $\frac{1}{4}W$	R405105
R206	1k0 $\pm 5\%$, $\frac{1}{4}W$	R405105
R207	10k $\pm 5\%$, $\frac{1}{4}W$	R405106
R208	330 $\pm 5\%$, $\frac{1}{4}W$	R405334
R209	10k $\pm 5\%$, $\frac{1}{4}W$	R405106
R210	120k $\pm 5\%$, $\frac{1}{4}W$	R405127
R211	4M7 $\pm 10\%$, $\frac{1}{4}W$	R405478
R212	120k $\pm 5\%$, $\frac{1}{4}W$	R405127
R213	1k2 $\pm 5\%$, $\frac{1}{4}W$	R401125
R214	470 $\pm 5\%$, $\frac{1}{4}W$	R401474

CIRCUIT REF.	DESCRIPTION	PART NO.
	RESISTORS (continued)	
R215	150 $\pm$ 5%, $\frac{1}{3}$ W	R401154
R216	220k $\pm$ 5%, $\frac{1}{3}$ W	R401227
R217	10k $\pm$ 5%, $\frac{1}{3}$ W	R405106
R218	68k $\pm$ 5%, $\frac{1}{3}$ W	R405686
RV1	Not fitted	—
RV2	4k7, variable	R492475
RV3	22k, variable	R492226
RV4	22k, variable	R492226
RV5	1k0, variable	R492105
RV6	4k7, variable	R492475
RV7	4k7, variable	R492475
RV8	100k, variable	R492107
RV9	100k, variable	R492107
	CONNECTORS	
SK1	Socket, 16-pin, DIL	R808016
SK2	Socket, 16-pin, DIL	R808016
SK3	Socket, 16-pin, DIL	R808016
SK4	2-part connector, 16 pins	R810016
SK5	2-part connector, 4 pins	R810004
SK6	2-part connector, 5 pins	R810005
SK7	2-part connector, 16 pins	R810016
SK8	2-part connector, 14 pins	R810014
SK9	2-part connector, 13 pins	R810013
SK10	2-part connector, 3 pins	R810003
	SWITCH	
SW1	Not fitted	—
	TRANSFORMERS	
T1	Type F	R650105
T2	Not fitted	—
	TRANSISTORS	
TR1	ZTX212AL	R348212
TR2	ZTX107L	R348107
TR3	ZTX107L	R348107
TR4	ZTX212AL	R348212

CIRCUIT REF.	DESCRIPTION	PART NO.
	TRANSISTORS (continued)	
TR5	ZTX212AL	R348212
TR6	ZTX212AL	R348212
TR7	MPS 6523	R334655
TR8	2N918	R300918
TR9	ZTX212AL	R348212
TR10	2N2219	R302219
TR11	2N2905	R30295
TR12	ZTX212AL	R348212
TR13	ZTX107L	R348107
TR14	ZTX107L	R348107
TR15	ZTX107L	R348107
TR16	ZTX212AL	R348212
TR17	ZTX212AL	R348212
TR18	ZTX107L	R348107
TR19	E176	R325176
TR20	ZTX107L	R348107
TR21	ZTX107L	R348107
TR22	ZTX212AL	R348212
TR23	ZTX107L	R348107
TR24	ZTX107L	R348107
TR25	ZTX107L	R348107
TR26	ZTX107L	R348107L
TR27	E421	R325421
TR28	ZTX212AL	R348212
TR29	ZTX107L	R348107
TR30	ZTX107L	R348107
TR31	ZTX107L	R348107
TR32	ZTX212AL	R348212
TR33	MPS6521	R334653
TR34	ZTX107L	R348107
TR35	ZTX212AL	R348212
TR36	ZTX107L	R348107
TR37	2N2369A	R312369
TR38	ZTX107L	R348107

CIRCUIT REF.	DESCRIPTION	PART NO.
	TRANSISTORS (continued)	
TR39	ZTX212AL	R348212
TR40	ZTX107L	R348107
TR41	ZTX107L	R348107
TR42	ZTX212AL	R348212
TR43	ZTX107L	R348107
TR44	ZTX107L	R348107
TR45	ZTX212AL	R348212
TR46	ZTX107L	R348107
TR47	ZTX107L	R348107
TR48	BFR41	R322041
TR49	BFR81	R322081
TR50	ZTX107L	R348107
TR51	BFR81	R322081
TR52	ZTX107L	R348107
TR53	ZTX212AL	R348212
TR54	ZTX212AL	R348212
TR55	78M12	R330784
TR56	E300	R325300
	CRYSTAL OSCILLATOR	
X1	8.8MHz	R695886

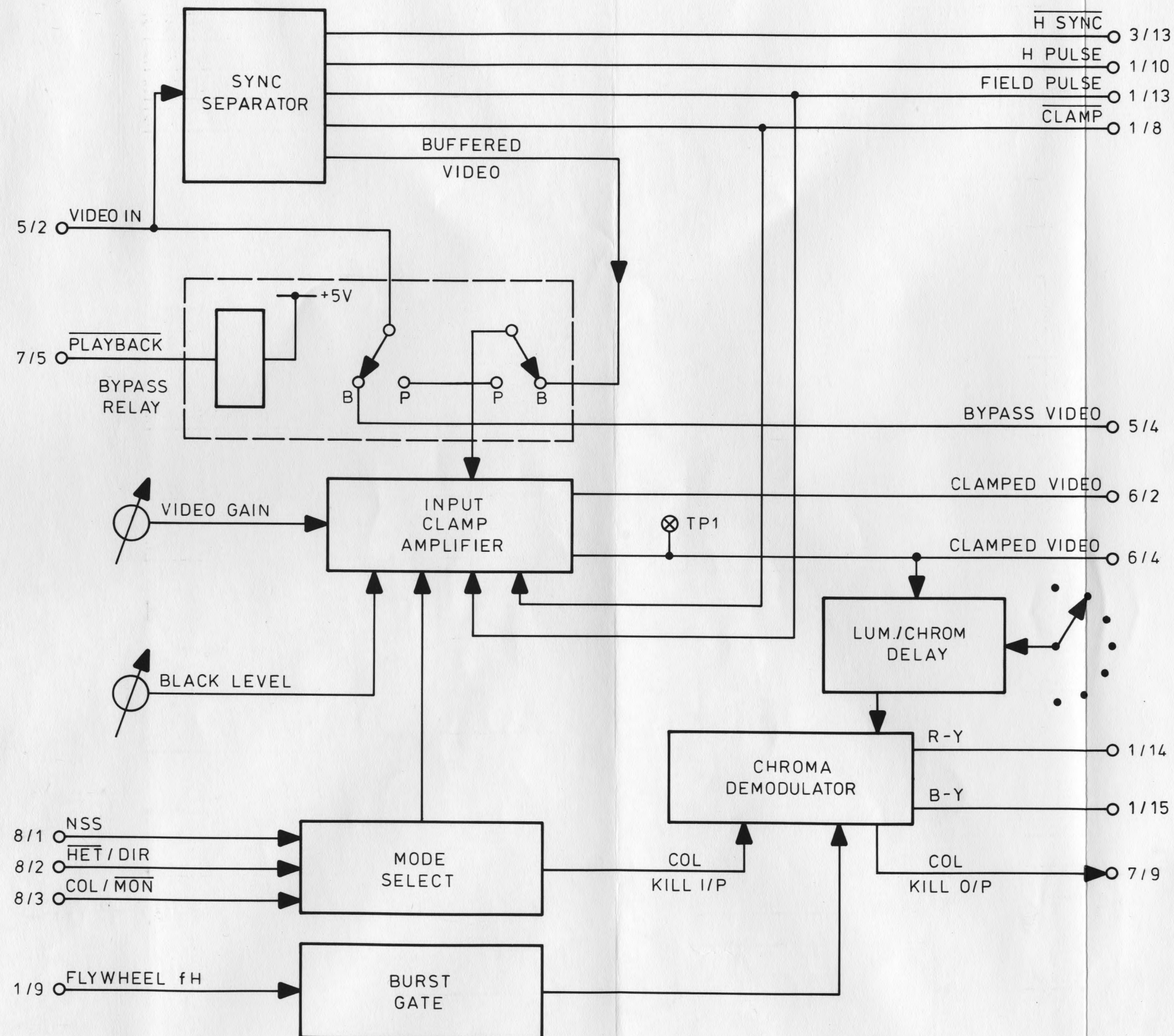
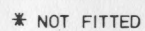


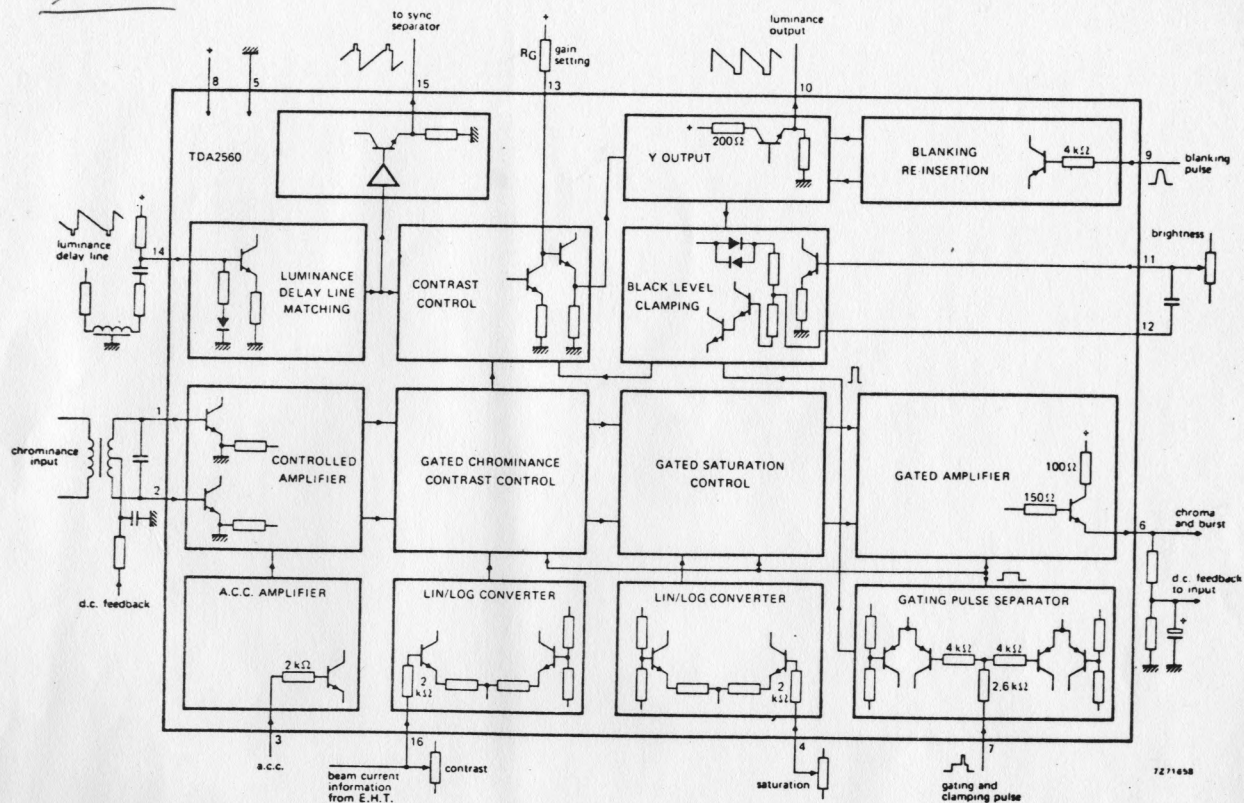
FIGURE 1 BLOCK DIAGRAM



IVC PCB GL206/FIG 2

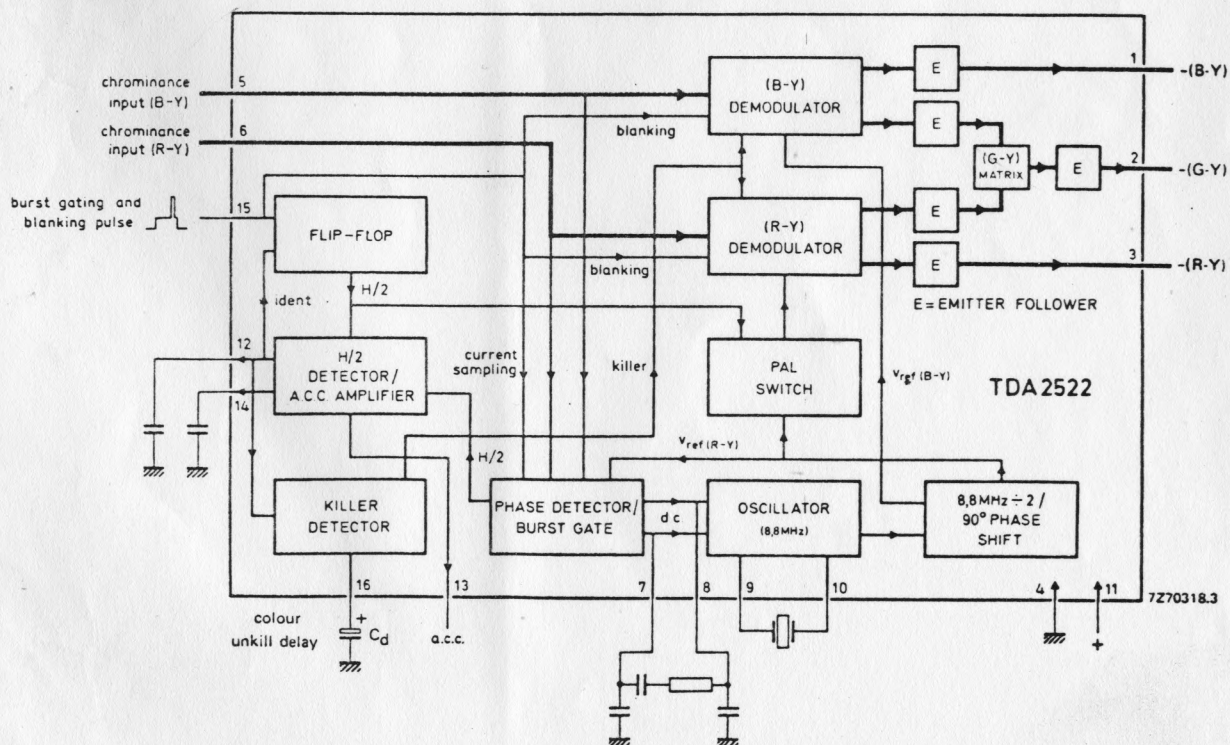
BLOCK DIAGRAM

TDA 2560



BLOCK DIAGRAM

TDA 2522



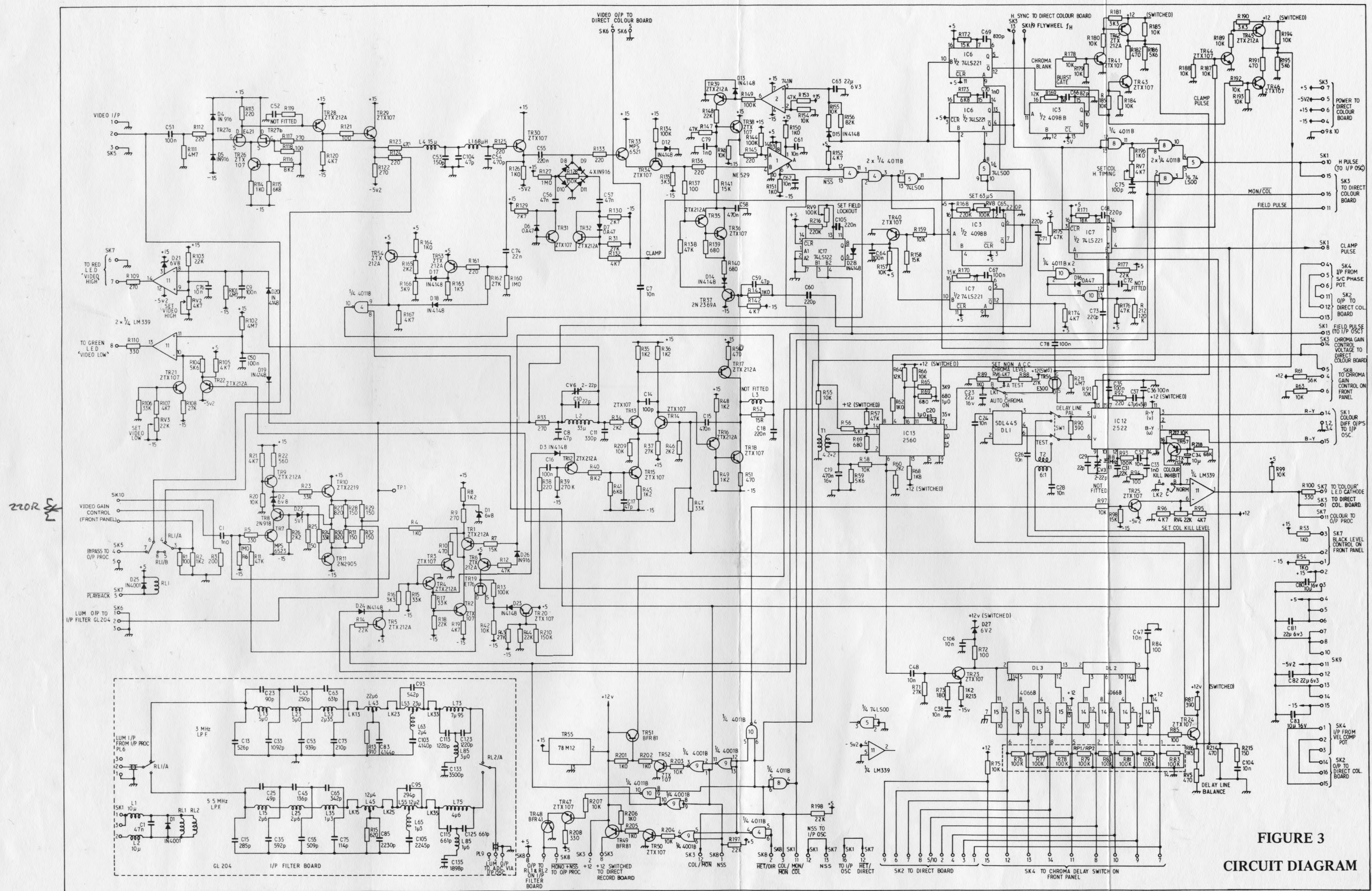


FIGURE 3
CIRCUIT DIAGRAM

INPUT OSCILLATOR
IVC PCB GL203

INTRODUCTION	1
CIRCUIT DESCRIPTION	1
ADJUSTMENTS	3
CONNECTIONS	3
TEST POINTS	4
COMPONENT SCHEDULE	5

FIGURE 1	OSCILLATOR CONTROL BLOCK DIAGRAM
FIGURE 2	LUMINANCE/CHROMINANCE TIMING CIRCUITS BLOCK DIAGRAM
FIGURE 3	COMPONENT LAYOUT
FIGURE 4	CIRCUIT DIAGRAM

INPUT OSCILLATOR

IVC PCB GL203

INTRODUCTION

The Input Oscillator card contains a voltage controlled 13.4MHz oscillator circuit and a triggered voltage controlled 14.4MHz oscillator circuit. The 13.4MHz oscillator is the VCO for the horizontal sync pulse "flywheel" phase-locked loop. The purpose of this loop is to generate an fH reference signal phase-locked to off tape horizontal sync pulses, and to produce burst gate timing pulses for the Input Processor card. The 14.4MHz oscillator includes a frequency control loop and provides the clock signals for the chrominance multiplexer and for the luminance and chrominance ADC's.

CIRCUIT DESCRIPTION

Horizontal Sync Pulse "Flywheel" Circuit

The 13.4MHz (858fH) voltage controlled oscillator consists of an ECL gate package (IC1). The output from the oscillator is converted to TTL level by IC2 whose output (monitored at TP5) clocks divide-by-13 counter IC3. The output at IC3/11 clocks the divide-by-66 circuit composed of dividers IC5 and IC6. The horizontal frequency square wave on IC6/13 is the FLYWHEEL fH burst reference signal and is output to the Input Processor on SK6/9. The signal is inverted at IC7/3, and both true and inverted signals are fed to the phase comparator circuit comprising the other three gates of IC7.

The other input to the phase comparator is derived from the separated horizontal sync pulse, H PULSE, input on SK6/10 from the Input Processor. The positive edges of the H PULSE trigger monostable IC9/2. The Q output from IC9/13 provides the fH TRIG output to the luminance and chrominance ADC cards (this is

not used in the ADC circuitry but is for test purposes only), and the $\bar{Q}$ output on pin 4 is applied to IC4/6.

The other input to IC4 on pin 5 is from link LK1. This either allows IC4/4 to enable the phase comparator continuously (in position B-C) or inhibits it during field blanking (in position A-B). The output of the phase comparator at the junction of R9 and R10 is connected via link LK2 (position A-B) to the varactor diode D1 through R1. Connecting LK2 to position B-C fixes the control voltage to the oscillator at 2.5V and opens the phase-locked loop for fault finding purposes. Components R9, R10, C3, C4, and R6 determine the loop time constant.

The action of the loop is to keep the negative edge of the FLYWHEEL fH square wave (monitored at TP12) centred on the pulse at IC4/4. The nominal control voltage on link LK2 is 2.5V, but final adjustment of L1 may be made in order to centre the burst gate signal produced on the Input Processor card about the incoming "off tape" burst. This is achieved by adjusting L1 for minimum chroma amplitude while observing the output of the TBC-2002 when it is fed with a colour bar input.

14.4MHz Oscillator Control Circuits

The 14.4MHz (924fH) oscillator consists of an ECL gate package (IC10) and is triggered from the H PULSE (input on SK6/10) via IC9.

The output from the oscillator provides the timing signals for the chrominance multiplexer circuits, and is also used to generate the chrominance and luminance clock signals required on the store and ADC cards.

A frequency control loop locks the pulsetrain output from the 14.4MHz oscillator in a fixed relationship with that from the 13.4MHz oscillator

(i.e. 924 to 858). The control loop comprises a balanced mixer (IC12) and phase comparator (IC14 and IC16/1,4 with switchable current sources TR1,2,3,4.).

The ECL inputs to the balanced mixer are derived from the 14.4MHz oscillator (IC12 pins 1 and 4) and the 13.4MHz oscillator (IC12 pins 8 and 10). The difference frequency at the output (IC12 pins 6 and 12) is at 1.03MHz (66fh) and is low-passed filtered by a balanced filter arrangement. The resultant 1.03MHz sync wave is converted to TTL level square wave at IC17/9 and connected to clock input IC14/3 in the phase comparator circuit.

The other clock input of the phase comparator (IC14/11) is from the divide-by-14 counter (IC13) which is clocked by the 14.4MHz TTL output from IC11/4. The output from the phase comparator circuit is filtered by C36, C37 and R57, and is fed via link LK3 to varactor diode D4 which controls the frequency of the 14.4MHz oscillator.

Positive-going fh STOP pulses to the 14.4MHz oscillator are coupled to IC10/4 from monostable IC9/5. This monostable is triggered when IC9/4 goes high (i.e. at the end of the fh TRIG pulse) and the period of the fh STOP pulse is normally 1 μ s. The negative-going fh STOP pulse from IC9/12 is output to the store card via SK5/11 and also clears IC15/1. This places a high on IC15/6 which inhibits the phase comparator by clearing IC14 pins 1 and 13, and also holds counter IC13 in its initial count state by setting IC16/11 high. At the end of the fh STOP pulse, IC15/2 returns high after a delay determined by R14 and C31. At the next positive edge from IC17/9 both IC13 and the phase comparator are released and the frequency control loop circuit operates normally.

Luminance/Chrominance Timing Circuits

The luminance signal from the Input Filter card is connected to the Input Oscillator card via SK3/21 and 22.

The chrominance U and V signals enter the Input Oscillator card either from the Input Processor card or the optional Direct Record card as determined by the position of the DIRECT COLOUR/HET switch on the front panel. With this switch in the HET position, SK6/16 is closed to ground so that relay RL1 is de-energised and selects the U and V inputs from the Input Processor. With the switch in the DIRECT COLOUR position, TR16 is switched on and RL1 is energised so that the U and V inputs from the Direct Record card are selected.

The selected U and V signals are connected to the clamping and demodulator circuits. As these

circuits are similar in each channel, the U channel only is described. The U input passes through emitter follower TR18 and C63 to the base of TR7A via R59. The collector of clamp transistor TR19 is also connected on this point. The base of TR19 is coupled via C65 to the CLAMP signal input on SK6/8, and the emitter is connected to the 6.2V reference rail. This reference voltage is generated by D13 and connected from voltage follower operational amplifier IC19/7.

A negative-going CLAMP pulse switches on clamp transistor TR19 and clamps the negative side of C63 to the 6.2V reference rail. The emitter follower TR7A drives the signal through a 1.5MHz low pass filter to the base of current source TR7B.

The collector of each current source TR7B (U Channel) and TR5B (V Channel) is driven by opposing fixed current sources TR10 and TR9. The difference currents are fed to the two inputs of the multiplexer: the U current to the junction of D8 and D10, and the V current to the junction of D9 and D11. The U and V currents are selected alternately by divide-by-four counter IC20.

This counter is clocked by the ECL pulsetrain from the 14.4MHz oscillator via a delay network L11, C55. Each time the oscillator is stopped, the pulse from IC10/2 resets the counter. The 3.6MHz and 3.6MHz square wave outputs on IC20 pins 14 and 15 steer the multiplexer between the U and V signals. If pin 15 (Q) is high relative to pin 14 ($\bar{Q}$), the V current is supplied through D11 and no current passes through D9. Thus the U current is supplied from the emitter of TR14B, and the multiplexer output at SK4/22 is the U signal. When IC20 pin 14 ($\bar{Q}$) is high relative to pin 15 (Q), the U current is supplied through D10 and the emitter of TR14B now supplies the V signal. Note that the U signal may be offset from the V signal at the multiplexer output by adjusting potentiometer RV1 to alter the current of the fixed current source TR10. (This potentiometer is used in setting the white balance).

The signals for steering the digital luminance and chrominance multiplexers on the ADC and Store cards are derived from divide-by-2 counter IC21. This counter is clocked by the 14.4MHz ECL pulsetrain, and is reset from IC10/2 when the 14.4MHz oscillator is stopped. The true and inverted 7.2MHz square waves from IC21 pins 15 and 14 are applied as clock signals to the chrominance ADC via SK4/26 and 27. These signals are also converted to TTL level of dual polarity by IC11/13 and 12, and output to the Store card as the CHROMA MPX clock (SK5/15) and the Y MPX clock (SK5/14).

Luminance ECL clocks for the Y ADC are selected by switching arrangement IC22 as determined by the MON/ $\bar{COL}$ signal on SK6/11. In

colour mode (SK6/11 low), 7.2MHz clocks are selected from IC21/15, and in monochrome mode (SK6/11 high) IC21 is held in a fixed state by a high on pin 12 and 14.4MHz clocks are selected from IC10/7. The selected clocks are output to the Y ADC via SK3/26 and 27.

ADJUSTMENTS

LK1 – Selects inhibit ON/OFF for the 13.4MHz phase-locked loop during the field period. Normally in the ON position (A–B). If field blanking is not required, it is connected in the OFF position (B–C).

LK2 – Opens or closes the control loop for the 13.4MHz oscillator. It is normally in the closed loop position (A–B). For open loop operation, it is changed to position B–C, and inductor L1 is adjusted to give 2.5V control voltage on LK2.

LK3 – Opens or closes the control loop for the 14.4MHz oscillator. It is normally in the closed loop position (A–B). For open loop operation, it is changed to position B–C, and inductor L2 is adjusted to give 5V control voltage on LK3.

LK4 – Allows the 4.4MHz oscillator to be triggered via the H PULSE. If it is required for test purposes that the oscillator operates continuously, this link is removed.

RV1 – Adjusts the B–Y white balance of the output chrominance during active picture time. It is adjusted in conjunction with the OFFSET control on the chrominance ADC card for white balance at the output of the TBC-2002.

L1 – Adjusts the free-running frequency of the 13.4MHz oscillator.

L2 – Adjusts the free-running frequency of the 14.4MHz triggered oscillator.

NOTE:— No attempt should be made to adjust inductors L3–L6 on this card.

CONNECTIONS

SK1 Digital Luminance Data Store Card.

1	YD1
2	YD2

3	YD3
4	YD4
5	YD5
6	YD6
7	YD7
8	YD8 (LSB)
9	YD8
10	YD7
11	YD6
12	YD5
13	YD4
15	YD2
16	YD1 (MSB)

SK2 Digital Chrominance Data to Store Card.

1	CD1
2	CD2
3	CD3
4	CD4
5	CD5
6	CD6
7	CD7
8	CD8 (LSB)
9	CD8
10	CD7
11	CD6
12	CD5
13	CD4
14	CD3
15	CD2
16	CD1 (MSB)

SK3 Connections to Luminance ADC Card.

1	Ground
3	YD8 (LSB)
4	YD8
5	YD7
6	YD7
7	YD6
8	YD6
9	YD5
10	YD5
11	YD4
12	YD4
13	YD3
14	YD3
15	YD2
16	YD2
17	YD1
18	YD1 (MSB)
19	–5.2V
20	+15V
21	Ground (LUM)

SK3 Connections to Luminance ADC Card.
(Continued)

22	LUM
25	+5V
26	LUM CKS (ECL) 7.2MHz or 14.4MHz
27	
30	Linked
31	
40	-15V
43	Ground

SK4 Connections to Chrominance ADC Card.

1	Ground
3	CD8
4	CD8
5	CD7
6	CD7
7	CD6
8	CD6
9	CD5
10	CD5
11	CD4
12	CD4
13	CD3
14	CD3
15	CD2
16	CD2
17	CD1
18	CD1
19	-5.2V
20	+15V
21	Ground
22	Multiplexed U,V signal
23	Ground
24	Ground
25	+5V
26	7.2MHz CLK (ECL)
27	7.2MHz CLK (ECL)
29	Linked
30	
38	fH TRIG
40	-15V
43	Ground

SK5 Store Card Signals.

1-6	Ground
7	AUTO/MANUAL (V PHASE)
8	MINIMUM V PHASE CONTROL
9	V PHASE CONTROL
10	MAXIMUM V PHASE CONTROL
11	fH STOP
12	FLYWHEEL fH

13	FIELD
14	Y MPX
15	CHROMA MPX
16	14.4MHz CKS (TTL)

SK6 Input Processor Card Signals.

2	Ground (U)
3	Ground (V)
8	CLAMP
9	FLYWHEEL fH
10	fH TRIG
11	MON/COL
12	NSS
13	FIELD
14	V
15	U
16	DIRECT/HET

SK7 Power Connections

2	+15V
3	0V
4,5,6	+5V
7,8,10	0V
11,12	-5V
13,14	0V
15	-15V

SK8 Optional Direct Record Card Signals.

1	Ground (U)
2	Ground (V)
14	DIRECT/HET
15	V
16	U

SK9 Luminance Signal from Input Filter Card.

2	Luminance
3	Ground

SK10 V PHASE Control Signals.

1	MAXIMUM V PHASE CONTROL
2	V PHASE CONTROL
3	MINIMUM V PHASE CONTROL
4	AUTO/MANUAL (V PHASE)
5	Ground

TEST POINTS

TP1	Earth
TP2	V signal
TP3	Earth
TP4	U signal
TP5	858fH PLL output (13.4MHz TTL)
TP6	Multiplexer drive signal (3.6MHz square-wave)
TP7	Multiplexed U,V signal
TP8	Earth
TP9	1MHz difference frequency
TP10	1MHz difference frequency
TP11	14.4MHz TTL write clocks
TP12	FLYWHEEL fH signal

CIRCUIT REF.	DESCRIPTION	PART NO.
	CAPACITORS	
C1	10pF, 63V	R511005
C2	220pF, 63V	R512215
C3	470nF, 63V	R524745
C4	47nF, 100V	R524736
C5	10nF, 25V	R501033
C6	10nF, 25V	R501033
C7	1200pF, 63V	R511225
C8	10nF, 25V	R501033
C9	10nF, 25V	R501033
C10	39pF, 63V	R513905
C12	22pF, 63V	R512205
C13	220pF, 63V	R512205
C14	150pF, 63V	R511515
C15	82pF, 63V	R518215
C16	10nF, 25V	R501033
C17	10nF, 25V	R501033
C18	10nF, 25V	R501033
C19	10nF, 25V	R501033
C20	10nF, 25V	R501033
C21	10nF, 25V	R501033
C22	10nF, 25V	R501033
C23	10 μ F, 16V	R541062
C24	22 μ F, 6.3V	R542261
C25	22 μ F, 6.3V	R542261
C26	10 μ F, 16V	R541062
C27	10nF, 25V	R501033
C28	10nF, 25V	R501033
C29	270pF, 63V	R512715
C30	270pF, 63V	R512715
C31	560pF, 63V	R515615
C32	10nF, 25V	R501033
C33	10nF, 25V	R501033
C34	10nF, 25V	R501033
C35	10nF, 25V	R501033

CIRCUIT REF.	DESCRIPTION	PART NO.
	CAPACITORS (continued)	
C36	470nF, 63V	R524745
C37	47nF, 100V	R524745
C38	10nF, 25V	R501033
C39	Not fitted	—
C40	220pF $\pm 2\%$, 63V	R512215
C41	820pF $\pm 2\%$, 63V	R518215
C42	150pF $\pm 2\%$, 63V	R511515
C43	1000pF $\pm 2\%$, 63V	R511025
C44	100pF $\pm 2\%$, 63V	R511015
C45	220pF $\pm 2\%$, 63V	R512215
C46	Not fitted	—
C47	820pF $\pm 2\%$, 63V	R518215
C48	150pF $\pm 2\%$, 63V	R511515
C49	1000pF $\pm 2\%$, 63V	R511025
C50	100pF $\pm 2\%$, 63V	R511015
C53	10nF, 25V	R501033
C54	10nF, 25V	R501033
C55	33pF, 63V	R513305
C56	33pF, 63V	R513305
C57	10nF, 25V	R501033
C58	10nF, 25V	R501033
C59	10nF, 25V	R501033
C60	10 μ F, 16V	R541062
C61	10nF, 25V	R501033
C62	10nF, 25V	R501033
C63	22 μ F, 6.3V	R542261
C64	22 μ F, 6.3V	R542261
C65	470nF $\pm 10\%$, 100V	R524736
C66	47nF $\pm 10\%$, 100V	R524736
C67	10 μ F, 16V	R541062
C68	Not fitted	—
C69	10nF, 25V	R501033
C70	10nF, 25V	R501033
C71	10nF, 25V	R501033

CIRCUIT REF.	DESCRIPTION	PART NO.
	CAPACITORS (continued)	
C72	10nF, 25V	R501033
C73	10nF, 25V	R501033
C74	10nF, 25V	R501033
C75	10nF, 25V	R501033
C76	10nF, 25V	R501033
C77	10nF, 25V	R501033
C78	10nF, 25V	R501033
	DIODES	
D1	BA102B	R372102
D2	1N4148	R354148
D3	1N4148	R354148
D4	BA102B	R372102
D5	0A47	R385047
D6	1N4148	R354148
D7	1N827	R350827
D8	HP2835	R378283
D9	HP2835	R378283
D10	HP2835	R378283
D11	HP2835	R378283
D12	1N4001	R354001
D13	1N827	R350827
D14	0A47	R385047
D15	1N821	R350821
	INTEGRATED CIRCUITS	
IC1	10109	R250109
IC2	NE529N	R280529
IC3	74LS161	R240161

CIRCUIT REF.	DESCRIPTION	PART NO.
INTEGRATED CIRCUITS (continued)		
IC4	74LS02	R240002
IC5	40163BP*	R260163
IC6	40163B*	R260163
IC7	4011B	R261011
IC9	74221	R210221
IC10	10105P	R250105
IC11	10125P	R250125
IC12	MC1496	R281496
IC13	74LS161	R240161
IC14	74LS74	R240074
IC15	74LS74	R240074
IC16	74LS02	R240002
IC17	710N	R280710
IC18	1458N-8	R281458
IC19	1458N-8	R281458
IC20	10131P	R250131
IC21	10131P	R250131
IC22	10102P	R250102
INDUCTORS		
L1	Type P	R600215
L2	Type R	R600217
L3	Type N	R600113
L4	Type M	R600112
L5	Type N	R600113
L6	Type M	R600112
L7	47 μ H	R620473
L8	47 μ H	R620473
L9	Type E	R600004
L10	Type E	R600004
L11	47 μ H	R620473

*Signetics or Fairchild only

CIRCUIT REF.	DESCRIPTION	PART NO.
RESISTORS		
R1	100k, $\frac{1}{3}W$, $\pm 5\%$	R401107
R2	1k0, $\frac{1}{3}W$, $\pm 5\%$	R401105
R3	22k, $\frac{1}{3}W$, $\pm 5\%$	R401226
R4	22k, $\frac{1}{3}W$, $\pm 5\%$	R401226
R5	4k7, $\frac{1}{3}W$, $\pm 5\%$	R401475
R6	3k9, $\frac{1}{3}W$, $\pm 5\%$	R401395
R7	1k0, $\frac{1}{3}W$, $\pm 5\%$	R401105
R8	4k7, $\frac{1}{3}W$, $\pm 5\%$	R401475
R9	4k7, $\frac{1}{3}W$, $\pm 5\%$	R401475
R10	4k7, $\frac{1}{3}W$, $\pm 5\%$	R401475
R11	1k0, $\frac{1}{3}W$, $\pm 5\%$	R401105
R12	1k0, $\frac{1}{3}W$, $\pm 5\%$	R401105
R13	10k, $\frac{1}{3}W$, $\pm 5\%$	R401106
R14	1k0, $\frac{1}{3}W$, $\pm 5\%$	R401105
R15	1k0, $\frac{1}{3}W$, $\pm 5\%$	R401105
R16	4k7, $\frac{1}{3}W$, $\pm 5\%$	R401475
R17	Not fitted	—
R18	1k0, $\frac{1}{3}W$, $\pm 5\%$	R401105
R19	270, $\frac{1}{3}W$, $\pm 5\%$	R401274
R21	100k, $\frac{1}{3}W$, $\pm 5\%$	R401107
R22	4k7, $\frac{1}{3}W$, $\pm 5\%$	R401475
R23	4k7, $\frac{1}{3}W$, $\pm 5\%$	R401475
R24	Not fitted	—
R25	4k7, $\frac{1}{3}W$, $\pm 5\%$	R401475
R26	1k0, $\frac{1}{3}W$, $\pm 5\%$	R401105
R27	10k, $\frac{1}{3}W$, $\pm 5\%$	R401106
R28	10k, $\frac{1}{3}W$, $\pm 5\%$	R401106
R29	1k0, $\frac{1}{3}W$, $\pm 5\%$	R401105
R30	1k0, $\frac{1}{3}W$, $\pm 5\%$	R401105
R31	1k0, $\frac{1}{3}W$, $\pm 5\%$	R401105
R32	10k, $\frac{1}{3}W$, $\pm 5\%$	R401106
R33	4k7, $\frac{1}{3}W$, $\pm 5\%$	R401475
R34	2k2, $\frac{1}{3}W$, $\pm 5\%$	R401225

CIRCUIT REF.	DESCRIPTION	PART NO.
RESISTORS (continued)		
R35	2k2, $\frac{1}{3}$ W, $\pm 5\%$	R401225
R36	220, $\frac{1}{3}$ W, $\pm 5\%$	R401224
R37	2k2, $\frac{1}{3}$ W, $\pm 5\%$	R401225
R38	100, $\frac{1}{3}$ W, $\pm 5\%$	R401104
R39	220, $\frac{1}{3}$ W, $\pm 5\%$	R401224
R40	100, $\frac{1}{3}$ W, $\pm 5\%$	R401104
R41	10k, $\frac{1}{3}$ W, $\pm 5\%$	R401106
R42	1k0, $\frac{1}{3}$ W, $\pm 5\%$	R401105
R43	2k2, $\frac{1}{3}$ W, $\pm 5\%$	R401225
R44	1k0, $\frac{1}{3}$ W, $\pm 5\%$	R401105
R45	Not fitted	—
R46	220, $\frac{1}{3}$ W, $\pm 5\%$	R401224
R47	220, $\frac{1}{3}$ W, $\pm 5\%$	R401224
R48	470, $\frac{1}{3}$ W, $\pm 5\%$	R401474
R49	1k0, $\frac{1}{3}$ W, $\pm 5\%$	R401105
R50	1k0, $\frac{1}{3}$ W, $\pm 5\%$	R401105
R51	1k0, $\frac{1}{3}$ W, $\pm 5\%$	R401105
R52	6k8, $\frac{1}{3}$ W, $\pm 5\%$	R401685
R53	560, $\frac{1}{3}$ W, $\pm 5\%$	R401564
R54	15k, $\frac{1}{3}$ W, $\pm 5\%$	R401156
R55	6k8, $\frac{1}{3}$ W, $\pm 5\%$	R401685
R56	3k8, $\frac{1}{3}$ W, $\pm 5\%$	R401335
R57	4k8, $\frac{1}{3}$ W, $\pm 5\%$	R401475
R58	270, $\frac{1}{3}$ W, $\pm 5\%$	R401274
R59	270, $\frac{1}{3}$ W, $\pm 5\%$	R401274
R60	470, $\frac{1}{3}$ W, $\pm 5\%$	R401474
R61	150, $\frac{1}{3}$ W, $\pm 5\%$	R401154
R62	470, $\frac{1}{3}$ W, $\pm 5\%$	R401474
R63	150, $\frac{1}{3}$ W, $\pm 5\%$	R401154
R64	560, $\frac{1}{3}$ W, $\pm 5\%$	R401564
R65	100, $\frac{1}{3}$ W, $\pm 5\%$	R401104
R66	330, 0.4W, $\pm 1\%$	R432334
R67	3k3, $\frac{1}{3}$ W, $\pm 5\%$	R401335

CIRCUIT REF.	DESCRIPTION	PART NO.
RESISTORS (continued)		
R68	1k0, $\frac{1}{3}$ W, $\pm 5\%$	R401105
R69	1k2, $\frac{1}{3}$ W, $\pm 5\%$	R401125
R70	100, $\frac{1}{3}$ W, $\pm 5\%$	R401104
R71	390, 0.4W, $\pm 1\%$	R432394
R72	1k5, 0.4W, $\pm 1\%$	R432155
R73	1k5, $\frac{1}{3}$ W, $\pm 5\%$	R401155
R74	100, $\frac{1}{3}$ W, $\pm 5\%$	R401104
R75	100, $\frac{1}{3}$ W, $\pm 5\%$	R401104
R76	1k5, 0.4W, $\pm 1\%$	R432155
R77	1k0, $\frac{1}{3}$ W, $\pm 5\%$	R401105
R78	1k0, $\frac{1}{3}$ W, $\pm 5\%$	R401105
R79	680, 0.4W, $\pm 1\%$	R432684
R80	390, 0.4W, $\pm 1\%$	R432394
R81	680, 0.4W, $\pm 1\%$	R432684
R82	330, 0.4W, $\pm 1\%$	R432334
R83	10k, 0.4W, $\pm 1\%$	R432106
R84	1k0, $\frac{1}{3}$ W, $\pm 5\%$	R401105
R85	1k0, $\frac{1}{3}$ W, $\pm 5\%$	R401105
R86	68R, $\frac{1}{3}$ W, $\pm 5\%$	R401683
R87	1k8, 0.4W, $\pm 1\%$	R432185
R88	1k0, $\frac{1}{3}$ W, $\pm 5\%$	R401105
R89	1k0, $\frac{1}{3}$ W, $\pm 5\%$	R401105
R90	10k, $\frac{1}{3}$ W, $\pm 5\%$	R401106
R91	4k7, $\frac{1}{3}$ W, $\pm 5\%$	R401475
R92	8k2, 0.4W, $\pm 1\%$	R432825
R93	2k2, $\frac{1}{3}$ W, $\pm 5\%$	R401225
R94	1k0, $\frac{1}{3}$ W, $\pm 5\%$	R401105
R95	1k0, $\frac{1}{3}$ W, $\pm 5\%$	R401105
R96	100, $\frac{1}{3}$ W, $\pm 5\%$	R401104
R97	100, $\frac{1}{3}$ W, $\pm 5\%$	R401104
R98	1k0, $\frac{1}{3}$ W, $\pm 5\%$	R401105
R99	1k0, $\frac{1}{3}$ W, $\pm 5\%$	R401105
R100	220k, $\frac{1}{3}$ W, $\pm 5\%$	R401227

CIRCUIT REF.	DESCRIPTION	PART NO.
	RESISTORS (continued)	
R101	220k, $\frac{1}{3}$ W, $\pm 5\%$	R401227
R102	6k8, 0.4W, $\pm 1\%$	R432685
R103	6k8, 0.4W, $\pm 1\%$	R432685
R104	680, 0.4W, $\pm 5\%$	R402684
R105	1k0, $\frac{1}{3}$ W, $\pm 5\%$	R401105
R106	1k0, $\frac{1}{3}$ W, $\pm 5\%$	R401105
R107	330, $\frac{1}{3}$ W, $\pm 5\%$	R401334
R108	75R, $\frac{1}{3}$ W, $\pm 5\%$	R401753
R109	4k7, $\frac{1}{3}$ W, $\pm 5\%$	R401475
R110	820, $\frac{1}{3}$ W, $\pm 5\%$	R401824
R111	4k7, $\frac{1}{3}$ W, $\pm 5\%$	R401475
RV1	100, $\pm 20\%$, variable	R490104
RV2	Not fitted	—
RV3	Not fitted	—
	RELAY	—
RL1	6V coil, 2-pole	R790062
	CONNECTORS	
SK1	Socket, 16-pin DIL	R808016
SK2	Socket, 16-pin DIL	R808016
SK3	Edge connector, 43-way	R809043
SK4	Edge connector, 43-way	R809043
SK5	Socket, 16-pin DIL	R808016
SK6	Socket, 16-pin DIL	R808016
SK7	2-part connector, 16-pin	R810016
SK8	Socket, 16-pin DIL	R808016
SK9	2-part connector, 3-pin	R810003
SK10	2-part connector, 5-pin	R810005
	TRANSISTORS	
TR1	BSX36	R322036
TR2	2N2369A	R312369

CIRCUIT REF.	DESCRIPTION	PART NO.
	TRANSISTORS (continued)	
TR3	2N2369A	R312369
TR4	2N2369A	R312369
TR5A	BC238B	R322238
TR5B	BC308B	R322308
TR7A	BC238B	R322238
TR7B	BC308B	R322308
TR9	ZTX107	R348107
TR10	ZTX107	R348107
TR11A,B	2N3806 or 2N3352	R303806 R303352
TR12	ZTX107	R348107
TR14A	BC308B	R322308
TR14B	BC238B	R322238
TR16	ZTX107	R348107
TR17	ZTX212A	R348212
TR18	ZTX212A	R348212
TR19	ZTX212A	R348212
TR20	ZTX212A	R348212
TR21	ZTX107	R348107

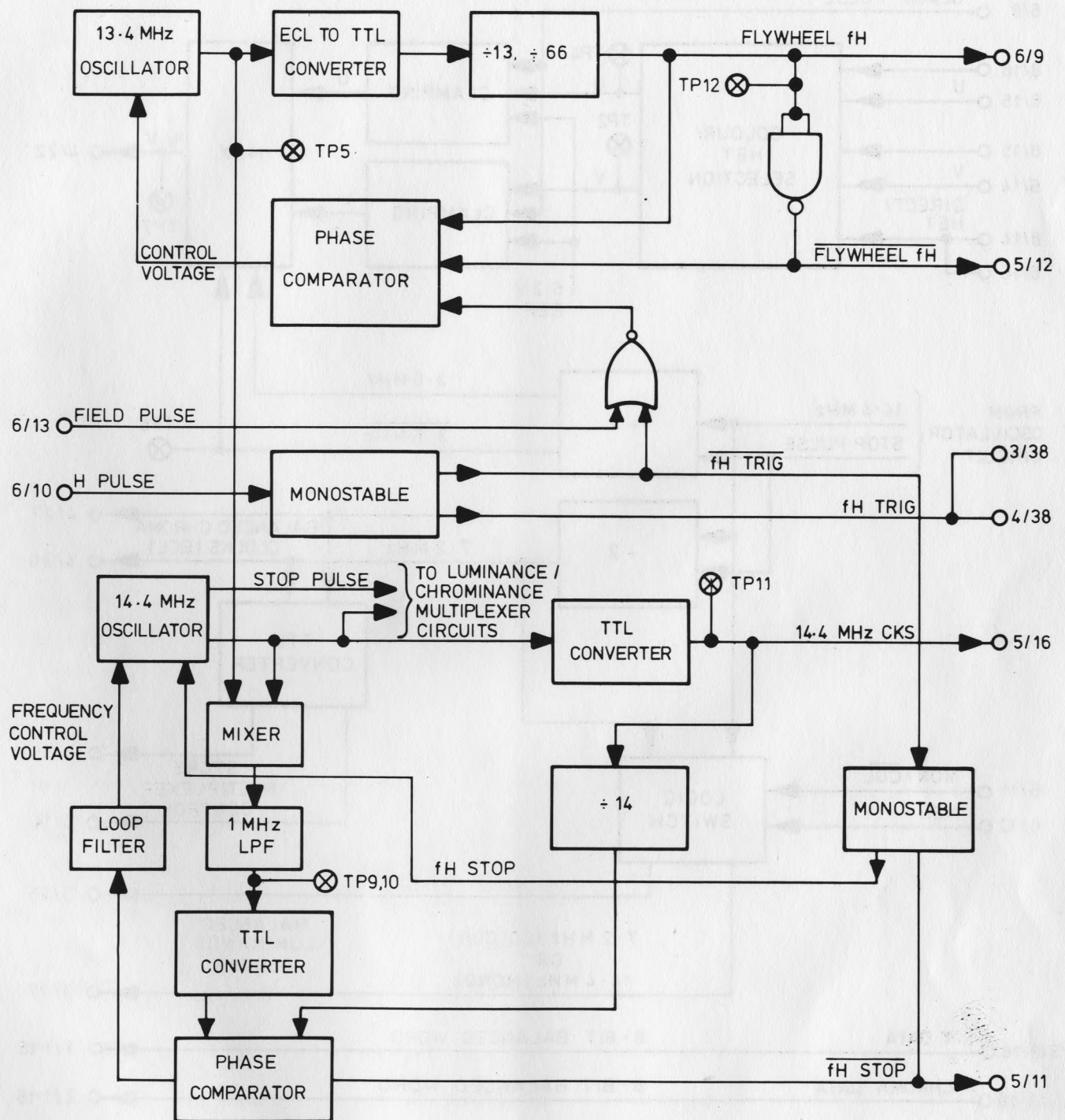


FIGURE 1 OSCILLATOR CONTROL BLOCK DIAGRAM

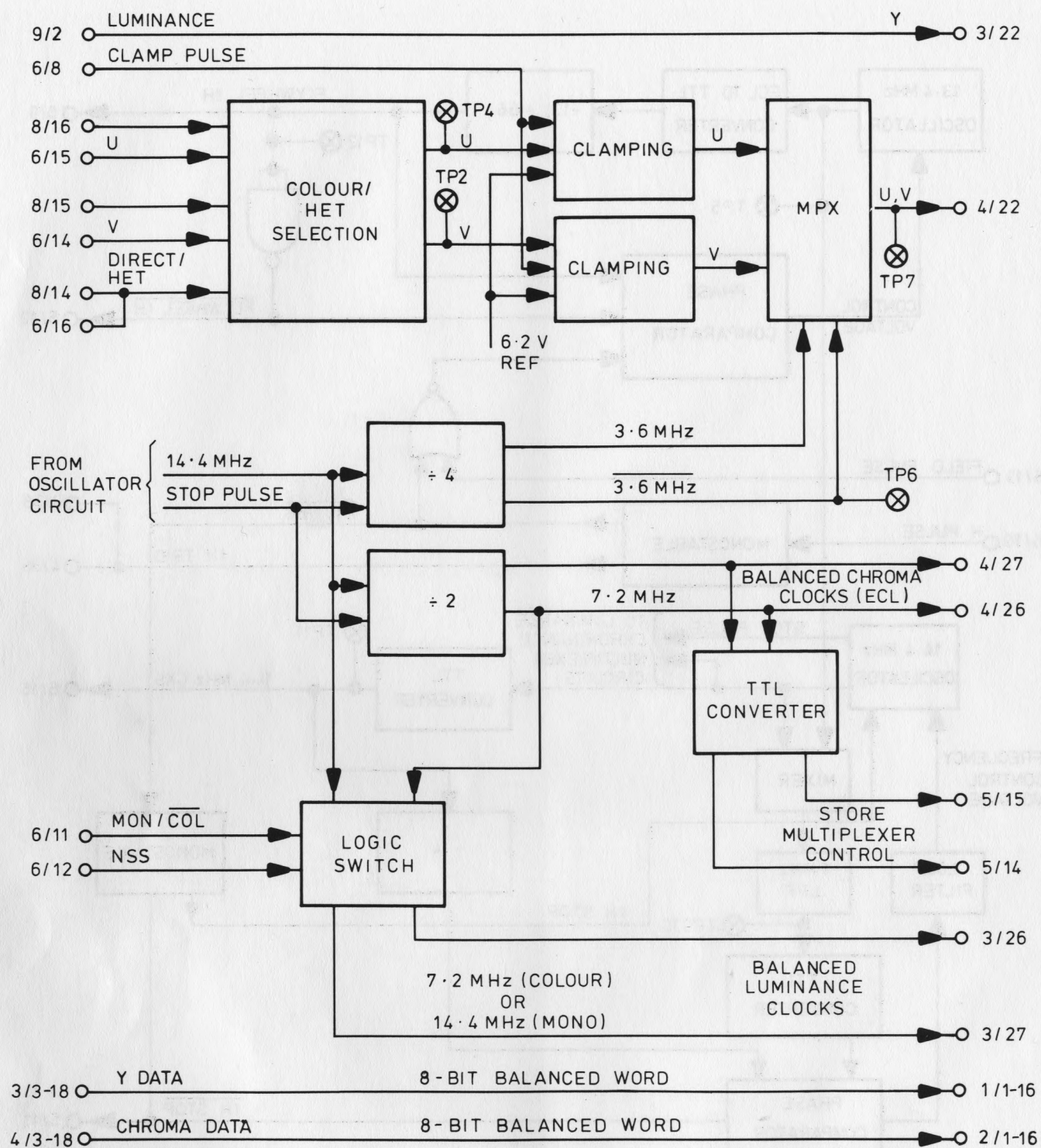
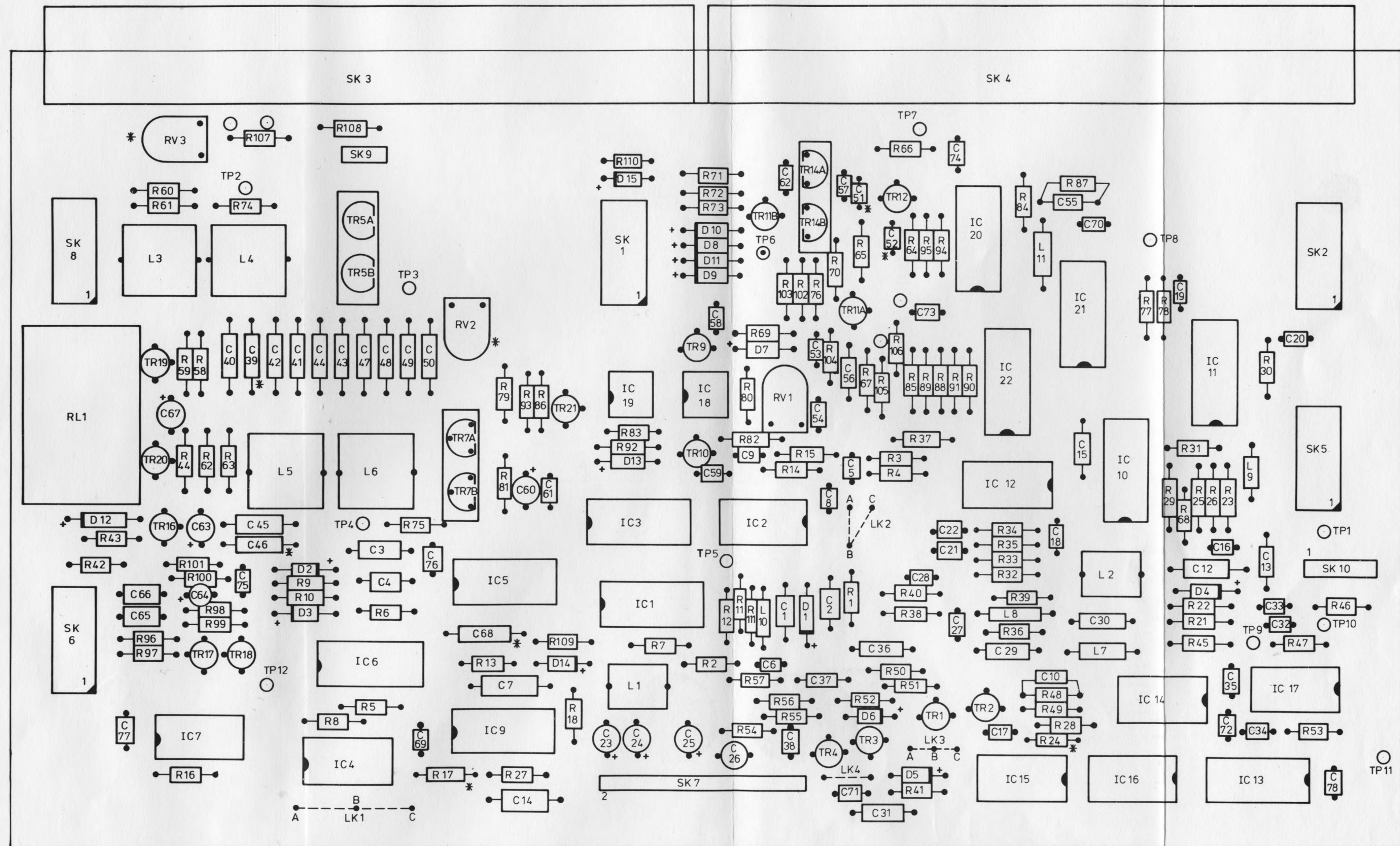


FIGURE 2 LUMINANCE/CHROMINANCE TIMING CIRCUITS
BLOCK DIAGRAM



* NOT FITTED

FIGURE 3 COMPONENT LAYOUT

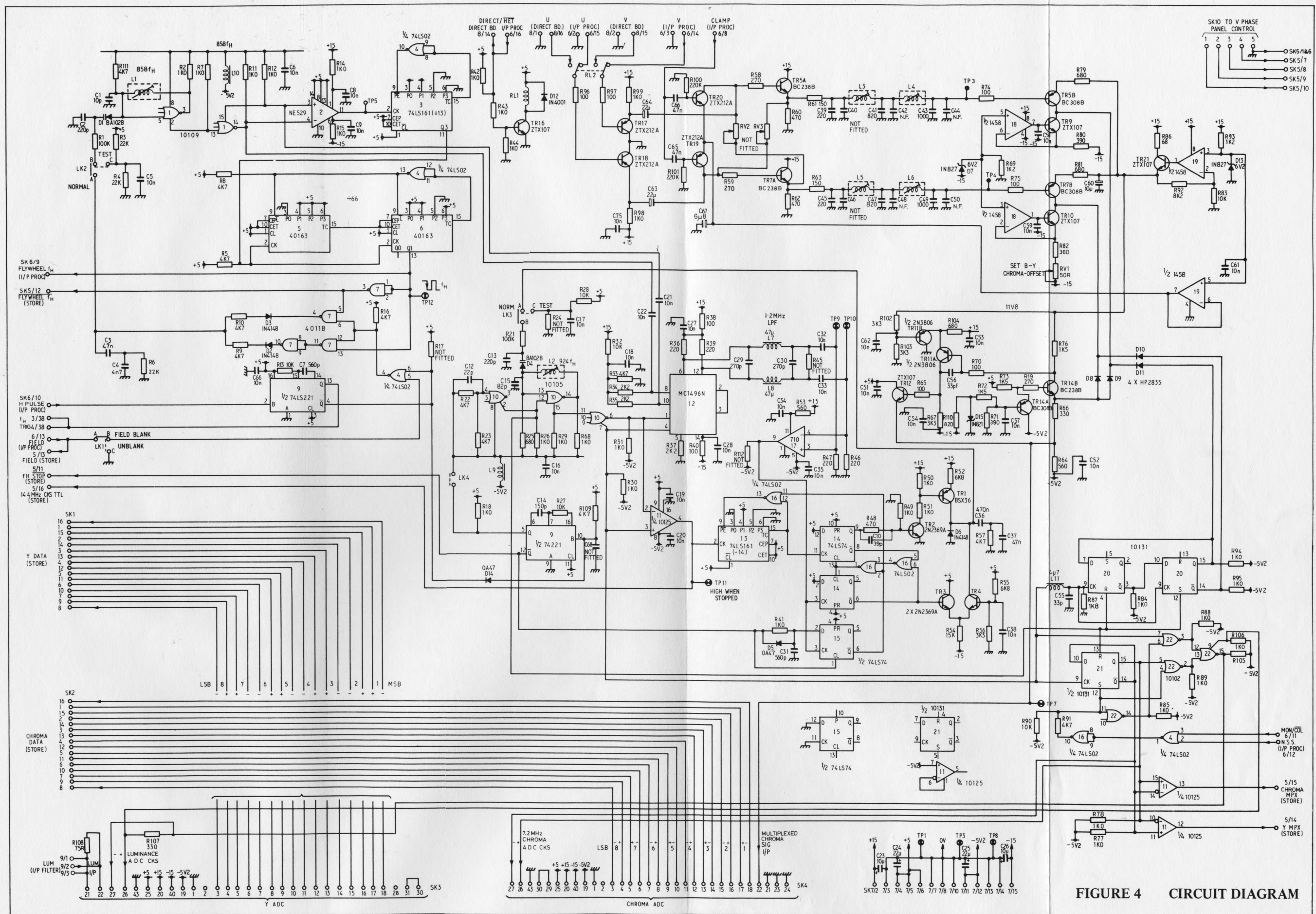


FIGURE 4 CIRCUIT DIAGRAM

**INPUT FILTER
IVC PCB GL204**

INTRODUCTION	1
CIRCUIT DESCRIPTION	1
ADJUSTMENTS	1
CONNECTIONS	1
TEST POINTS	1
COMPONENT SCHEDULE	2

FIGURE 1 COMPONENT LAYOUT

(NB The circuit diagram for this card is included on the circuit diagram for the Input Processor card)

INPUT FILTER IVC PCB GL204

INTRODUCTION

The Input Filter card contains two low pass filters with their associated group delay correctors.

CIRCUIT DESCRIPTION

The circuit diagram for the Input Filter card is included on the Input Processor card circuit diagram.

The LUM input from the Input Processor card is connected via co-axial cable to PL6, and is connected to the 3MHz LPF for colour operation, or to the 5.5MHz LPF for monochrome. The appropriate filter is selected by two single pole relays, RL1 and RL2, which are mounted on the card. The relay coils are connected in parallel. One end is connected to the +5V rail via SK1/1 and 3 on the Input Filter card and SK8/8 on the Input Processor card. They are controlled by the MONO + NSS signal from the Input Processor card. The filtered output LUM signal is taken to the Input Oscillator card via PL9.

Six links are provided for testing the filter and equalising circuits.

ADJUSTMENTS

There are no adjustments on this card. No attempt should be made to readjust these filters in the field.

CONNECTIONS

PL6 Luminance Input

1 Earth
2 LUM

PL9 Luminance Output

1 Earth
2 LUM

SK1 Relay connections

1,3 +5V
2 MONO + NSS

TEST POINTS

There are no test points on this card.

CIRCUIT REF.	DESCRIPTION	PART NO.
	CAPACITOR	
C1	47nF $\pm$ 20%, 100V	R524736
	DIODE	
D1	1N4001	R354001
	INDUCTORS	
L1	10 μ H	R620103
L2	10 μ H	R620103
	RELAYS	
RL1	5V coil	R790015
RL2	5V coil	R790015
	CONNECTOR	
SL1	2-part connector, 3 pins	R810003
	3MHz FILTER	
C13		R530526
C23		R530090
C33		R531092
C43		R530250
C53		R530939
C63		R530631
C73		R530210
C83		R534114
C93		R530542
C103		R534140
C113		R531220
C123		R531220
C133		R533500
L13	Type Z	R600325
L23	Type Z	R600325
L33	Type S	R600318
L43	Type AD	R600329
L53	Type AD	R600329
L63	Type AA	R600326
L73	Type AB	R600327
L83	Type AC	R600328

CIRCUIT REF.	DESCRIPTION	PART NO.
R13	3MHz FILTER (continued) 910 $\pm$ 2%, $\frac{1}{3}$ W	R441914
	5.5MHz FILTER	
C15		R530285
C25		R530049
C35		R530592
C45		R530136
C55		R530509
C65		R530342
C75		R530114
C85		R532230
C95		R530294
C105		R532245
C115		R530661
C125		R530661
C135		R531898
L15	Type S	R600318
L25	Type S	R600318
L35	Type T	R600319
L45	Type Y	R600324
L55	Type Y	R600324
L65	Type V	R600321
L75	Type W	R600322
L85	Type X	R600323
R15	620 $\pm$ 2%, $\frac{1}{3}$ W	R441624

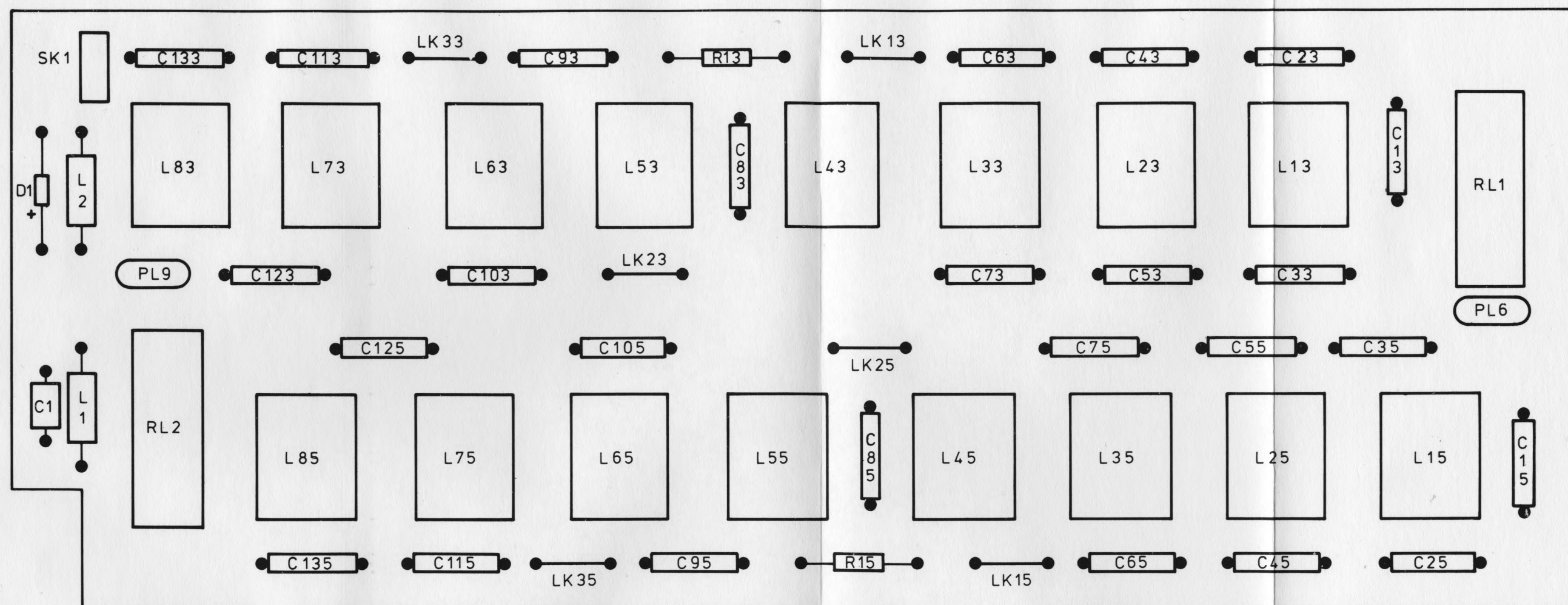


FIGURE 1 COMPONENT LAYOUT

ADC

**ANALOGUE TO DIGITAL CONVERTOR
IVC PCB GL217**

INTRODUCTION	1
CIRCUIT DESCRIPTION	1
ADJUSTMENTS	2
CONNECTIONS	2
TEST POINTS	2
COMPONENT SCHEDULE	3

FIGURE 1	BLOCK DIAGRAM
FIGURE 2	COMPONENT LAYOUT
FIGURE 3	CIRCUIT DIAGRAM

ANALOGUE TO DIGITAL CONVERTOR

IVC PCB GL217

INTRODUCTION

The TBC2002 contains two identical Analogue-to-Digital Convertor (ADC) cards GL217; one for converting the multiplexed chrominance analogue signal to 8-bit balanced digital data, and the other for similarly converting the luminance analogue signal. Each card contains a TRW type TDC1007J ADC integrated circuit (IC1) which is housed in a 64-pin DIL package. As the input and output signals for each card are at ECL level, and IC1 has TTL compatible data outputs and clock input, the other digital integrated circuits act as an interface between TTL and ECL levels. Moreover, the analogue input to IC1 is highly capacitive (approximately 300pF) and therefore a buffer amplifier circuit is included on each card with GAIN and OFFSET adjustments.

CIRCUIT DESCRIPTION

Input Amplifier

The analogue input signal enters the card on edge connector SK1/22 and is connected to the base of TR2a via base stopper R4. Transistors TR2a and TR2b are connected as a long-tailed pair with current source TR3. The collector of TR2b is connected to the collector of opposing current source TR6 and the cathode of Zener diode D2. The anode of D2 is connected to the base of TR8 and, through Zener diode D3, TR9. TR8 and TR9 are complementary emitter followers with current source TR7, and their outputs are via R23 and R24 respectively. Negative feedback is taken via R21, R22 and R11 to the base of TR2b.

The amplifier has a gain of 2 which is set by RV12 in series with R9 to ground. Because the input voltage range of IC1 is 0V to -2V, while the input voltage range at SK1/22 is +1V to 0V, it is necessary for a dc offset to be applied to the input

amplifier circuit. This offset is obtained by current source TR4 feeding the junction of R9 and R11, and is adjusted by RV8.

Zener diode D1 acts as the dc reference for the ADC card. It is fed with a current source TR1, and a further current source, TR5, "mirrors" the voltage of D1 across R13. Current source TR10 produces a 2V reference across R28, referred to 0V, and this -2V reference is buffered by IC10 and TR11 to provide a low impedance reference for IC1 (on pin 22). IC8 removes the temperature dependence of the base emitter voltage of all sources except TR1 and TR3.

The output of the amplifier circuit is monitored at TP2, and TR12 is a protection device to ensure that it does not exceed 0.7V above ground. Should this occur, TR12 conducts and clamps the cathode of D2 to ground thus reducing the amplifier output voltage. Similarly TR13 ensures that the output voltage cannot drop below -2.7V by clamping the anode of D3 to -2V if this occurs.

Components C6, C35 and R65 form a frequency response shaping circuit to minimise the settling time of the input amplifier.

Analogue-to-Digital Convertor IC1

The analogue input signal is applied to IC1 on pins 13, 15, 16, 18 and 20, and the -2V reference is applied on pin 22.

TTL level clock pulses enter on pin 30 and conversion occurs on the positive-going clock edge.

The data output is at TTL level and appears on pins 32 (LSB) to 40 (MSB).

Clock Pulse and Data Interfaces

The balanced ECL clock pulses from the Input Oscillator card are input to the ADC card on SK1/26 and 27. They connect to ECL line receiver IC9/4 and 5 and also to comparator IC7 which

provides TTL output. The TTL level clocks from IC7/10 (monitored at TP4) are used to clock IC1, and the ECL level clocks from IC9/7 (monitored at TP5) are used to clock the data output latches.

The TTL level data outputs from IC1 are connected to 8-bit D-type latch IC2. The enable pin for this latch (pin 11) is connected to +5V so that the latch is transparent and acts as a driver for the interface resistors R32 to R47. The resistor pairs (R32, R40; R33, R41; etc.) convert the TTL levels to ECL levels which are then connected to the inputs of D-type master-slave latches IC3 to IC6. The complementary ECL level outputs from these latches are output from the ADC card via edge connector SK1.

ADJUSTMENTS

RV8 — OFFSET: adjusts the dc level of the input amplifier circuit to IC1.

RV12 — GAIN: adjusts the gain of the input amplifier circuit to IC1.

NOTE

Under no circumstances should any attempt be made to adjust other components on this card. If its operation is suspect the card should be returned to IVC or their agents for repair.

CONNECTIONS

SK1	Edge connector pins
1	Digital ground
2	-5.2V
3	Bit 8 (LSB)
4	Bit 8
5	Bit 7
6	Bit 7
7	Bit 6
8	Bit 6
9	Bit 5
10	Bit 5
11	Bit 4
12	Bit 4
13	Bit 3
14	Bit 3
15	Bit 2
16	Bit 2
17	Bit 1
18	Bit 1 (MSB)
19	-5.2V
20	+15V
21,22	Analogue signal input
23,24	Analogue ground
25	+5V
26,27	ECL clock input
40	-15V

Digital
Data
Output

SK2	Power connections
1	Analogue ground
2	-6V
3	Analogue ground

TEST POINTS

TP1	Video input
TP2	Amplifier output
TP3	-2V VRB reference voltage
TP4	TTL level clocks
TP5	ECL level clocks

CIRCUIT REF.	DESCRIPTION	PART NO.
	CAPACITORS	
C1	10 μ F, 16V	R541062
C2	10 μ F, 16V	R541062
C3	10 μ F, 16V	R541062
C4	22 μ F, 6.3V	R542261
C5	22 μ F, 6.3V	R542261
C6	33pF, 63V	R513305
C7	10nF, 25V	R501033
C8	10nF, 25V	R501033
C9	10nF, 25V	R501033
C10	10 μ F, 16V	R541062
C11	Not fitted	—
C12	Not fitted	—
C13	10 μ F, 16V	R541062
C14	10 μ F, 16V	R541062
C15	10nF, 25V	R501033
C16	15pF, 63V	R501505
C17	15pF, 63V	R501505
C18	15pF, 63V	R501505
C19	15pF, 63V	R501505
C20	15pF, 63V	R501505
C21	15pF, 63V	R501505
C22	15pF, 63V	R501505
C23	15pF, 63V	R501505
C24	10 μ F, 16V	R541062
C25	22 μ F, 6.3V	R542261
C26	10 μ F, 16V	R541062
C27	10nF, 25V	R501033
C28	22 μ F, 6.3V	R542261
C29	10nF, 25V	R501033
C30	10 μ F, 16V	R541062
C31	10nF, 25V	R501033
C32	10nF, 25V	R501033
C33	10nF, 25V	R501033
C34	10nF, 25V	R501033

CIRCUIT REF.	DESCRIPTION	PART NO.
	CAPACITORS (continued)	
C35	100pF, 63V	R511015
C36	10nF, 25V	R501033
C37	10nF, 25V	R501033
	DIODES	
D1	1N827	R350827
D2	3.3V	R399332
D3	5.6V	R399562
	INTEGRATED CIRCUITS	
IC1	TDC1007J	R281007
IC2	74S373	R230373
IC3	10131	R250131
IC4	10131	R250131
IC5	10131	R250131
IC6	10131	R250131
IC7	760	R280760
IC8	LM324	R280324
IC9	10114	R250114
IC10	741	R280741
	RESISTORS	
R1	820 $\pm$ 1%, 0.4W	R432824
R2	Not fitted	—
R3	100 $\pm$ 5%, $\frac{1}{3}$ W	R401104
R4	33R $\pm$ 5%, $\frac{1}{3}$ W	R401333
R5	100 $\pm$ 5%, $\frac{1}{3}$ W	R401104
R6	560 $\pm$ 1%, 0.4W	R432564
R7	330 $\pm$ 1%, 0.4W	R432334
R9	82R $\pm$ 1%, 0.4W	R432823
R10	100 $\pm$ 5%, $\frac{1}{3}$ W	R401104
R11	22R $\pm$ 1%, 0.4W	R432223
R13	2k2 $\pm$ 1%, 0.4W	R432225
R14	100R $\pm$ 5%, $\frac{1}{3}$ W	R401104
R15	2k2 $\pm$ 1%, 0.4W	R432225
R16	100 $\pm$ 5%, $\frac{1}{3}$ W	R401104
R17	100 $\pm$ 5%, $\frac{1}{3}$ W	R401104
R18	560 $\pm$ 1%, 0.4W	R432564

CIRCUIT REF.	DESCRIPTION	PART NO.
	RESISTORS (continued)	
R19	1k2 $\pm$ 1%, 0.4W	R432125
R20	47R $\pm$ 5%, $\frac{1}{3}$ W	R401473
R21	220 $\pm$ 1%, 0.4W	R432224
R22	220 $\pm$ 1%, 0.4W	R432224
R23	68R $\pm$ 1%, 0.4W	R432683
R24	68R $\pm$ 1%, 0.4W	R432683
R25	47R $\pm$ 5%, $\frac{1}{3}$ W	R401473
R26	100 $\pm$ 5%, $\frac{1}{3}$ W	R401104
R27	1k0 $\pm$ 5%, $\frac{1}{3}$ W	R401105
R28	2k2 $\pm$ 1%, 0.4W	R432225
R29	6k8 $\pm$ 1%, 0.4W	R432685
R30	100 $\pm$ 5%, $\frac{1}{3}$ W	R401104
R31	1k0 $\pm$ 5%, $\frac{1}{3}$ W	R401105
R32	2k2 $\pm$ 5%, $\frac{1}{3}$ W	R401225
R33	2k2 $\pm$ 5%, $\frac{1}{3}$ W	R401225
R34	2k2 $\pm$ 5%, $\frac{1}{3}$ W	R401225
R35	2k2 $\pm$ 5%, $\frac{1}{3}$ W	R401225
R36	2k2 $\pm$ 5%, $\frac{1}{3}$ W	R401225
R37	2k2 $\pm$ 5%, $\frac{1}{3}$ W	R401225
R38	2k2 $\pm$ 5%, $\frac{1}{3}$ W	R401225
R39	2k2 $\pm$ 5%, $\frac{1}{3}$ W	R401225
R40	2k7 $\pm$ 5%, $\frac{1}{3}$ W	R401275
R41	2k7 $\pm$ 5%, $\frac{1}{3}$ W	R401275
R42	2k7 $\pm$ 5%, $\frac{1}{3}$ W	R401275
R43	2k7 $\pm$ 5%, $\frac{1}{3}$ W	R401275
R44	2k7 $\pm$ 5%, $\frac{1}{3}$ W	R401275
R45	2k7 $\pm$ 5%, $\frac{1}{3}$ W	R401275
R46	2k7 $\pm$ 5%, $\frac{1}{3}$ W	R401275
R47	2k7 $\pm$ 5%, $\frac{1}{3}$ W	R401275
R48	1k0 $\pm$ 5%, $\frac{1}{3}$ W	R401105
R49	1k0 $\pm$ 5%, $\frac{1}{3}$ W	R401105
R50	1k0 $\pm$ 5%, $\frac{1}{3}$ W	R401105
R51	1k0 $\pm$ 5%, $\frac{1}{3}$ W	R401105
R52	1k0 $\pm$ 5%, $\frac{1}{3}$ W	R401105
R53	1k0 $\pm$ 5%, $\frac{1}{3}$ W	R401105

CIRCUIT REF.	DESCRIPTION	PART NO.
	RESISTORS (continued)	
R54	1k0 $\pm$ 5%, $\frac{1}{3}$ W	R401105
R55	1k0 $\pm$ 5%, $\frac{1}{3}$ W	R401105
R56	1k0 $\pm$ 5%, $\frac{1}{3}$ W	R401105
R57	1k0 $\pm$ 5%, $\frac{1}{3}$ W	R401105
R58	1k0 $\pm$ 5%, $\frac{1}{3}$ W	R401105
R59	1k0 $\pm$ 5%, $\frac{1}{3}$ W	R401105
R60	1k0 $\pm$ 5%, $\frac{1}{3}$ W	R401105
R61	1k0 $\pm$ 5%, $\frac{1}{3}$ W	R401105
R62	1k0 $\pm$ 5%, $\frac{1}{3}$ W	R401105
R63	1k0 $\pm$ 5%, $\frac{1}{3}$ W	R401105
R64	330 $\pm$ 5%, $\frac{1}{3}$ W	R401334
R65	390 $\pm$ 5%, $\frac{1}{3}$ W	R401394
R66	100 $\pm$ 5%, $\frac{1}{3}$ W	R401104
R67	100 $\pm$ 5%, $\frac{1}{3}$ W	R401104
R68	100 $\pm$ 5%, $\frac{1}{3}$ W	R401104
R69	100 $\pm$ 5%, $\frac{1}{3}$ W	R401104
RV8	1k0, variable	R491105
RV12	100, variable	R491104
	CONNECTORS	
SK1	Edge connector, 43-pin	—
SK2	2-part connector, 3-way	R810003
	TRANSISTORS	
TR1	ZTX107	R348107
TR2a,b	MD8001	R338001
TR3	ZTX107	R348107
TR4	ZTX212	R348212
TR5	ZTX212	R348212
TR6	ZTX212	R348212
TR7	ZTX107	R348107
TR8	2N2219	R302219
TR9	2N2905	R302905
TR10	ZTX107	R348107
TR11	2N4037	R304037
TR12	ZTX107	R348107
TR13	ZTX212	R348212

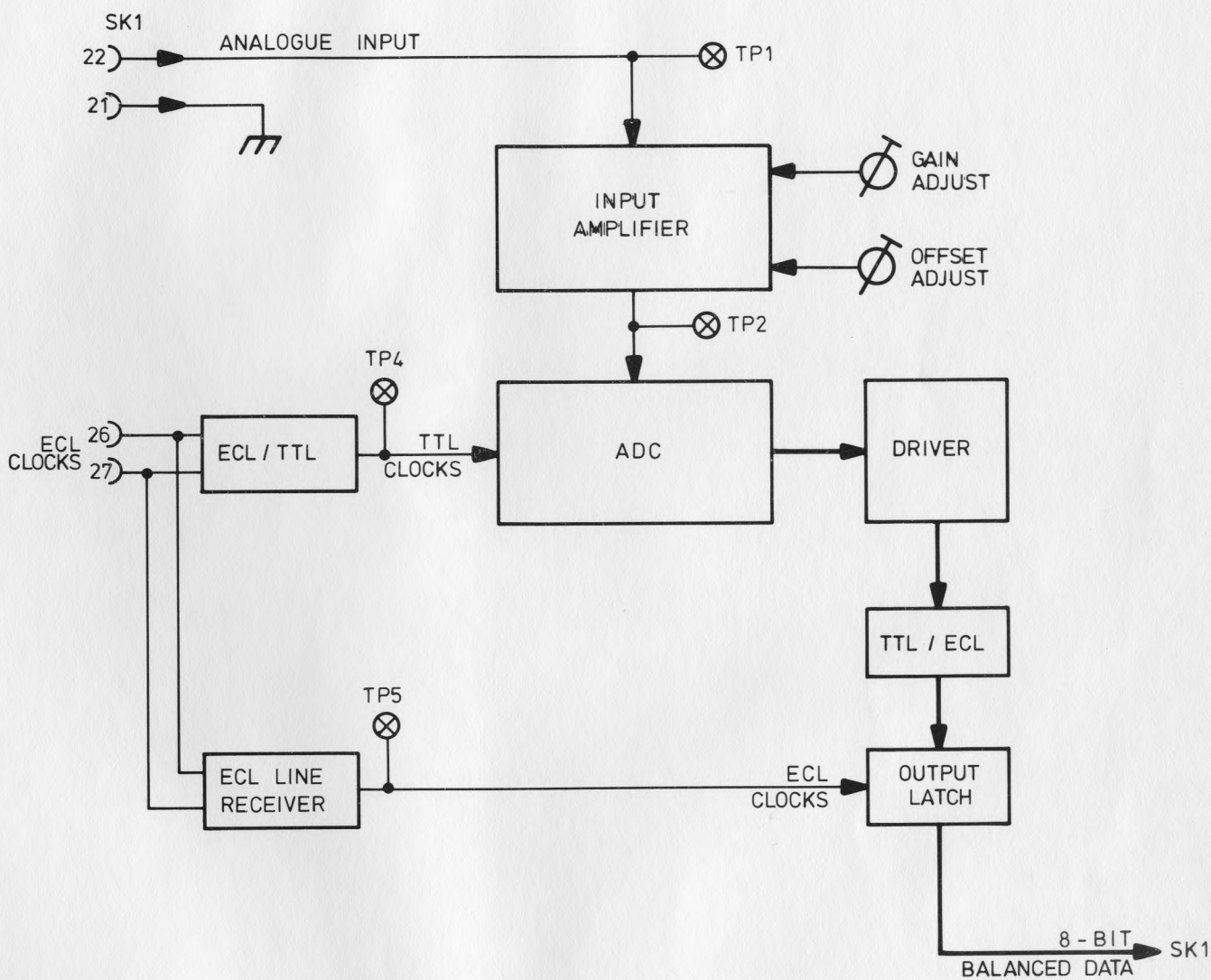


FIGURE 1 BLOCK DIAGRAM

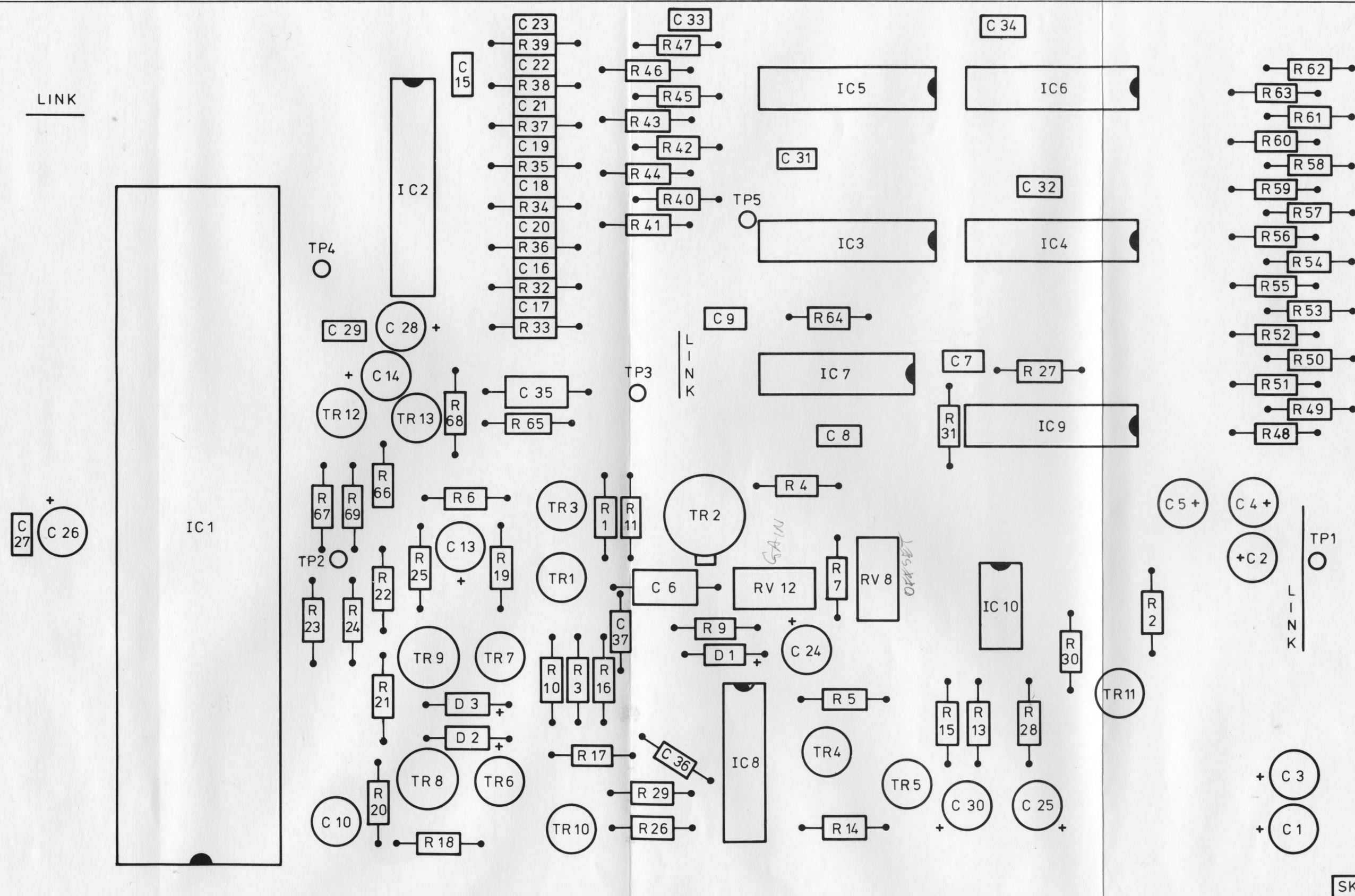


FIGURE 2 COMPONENT LAYOUT

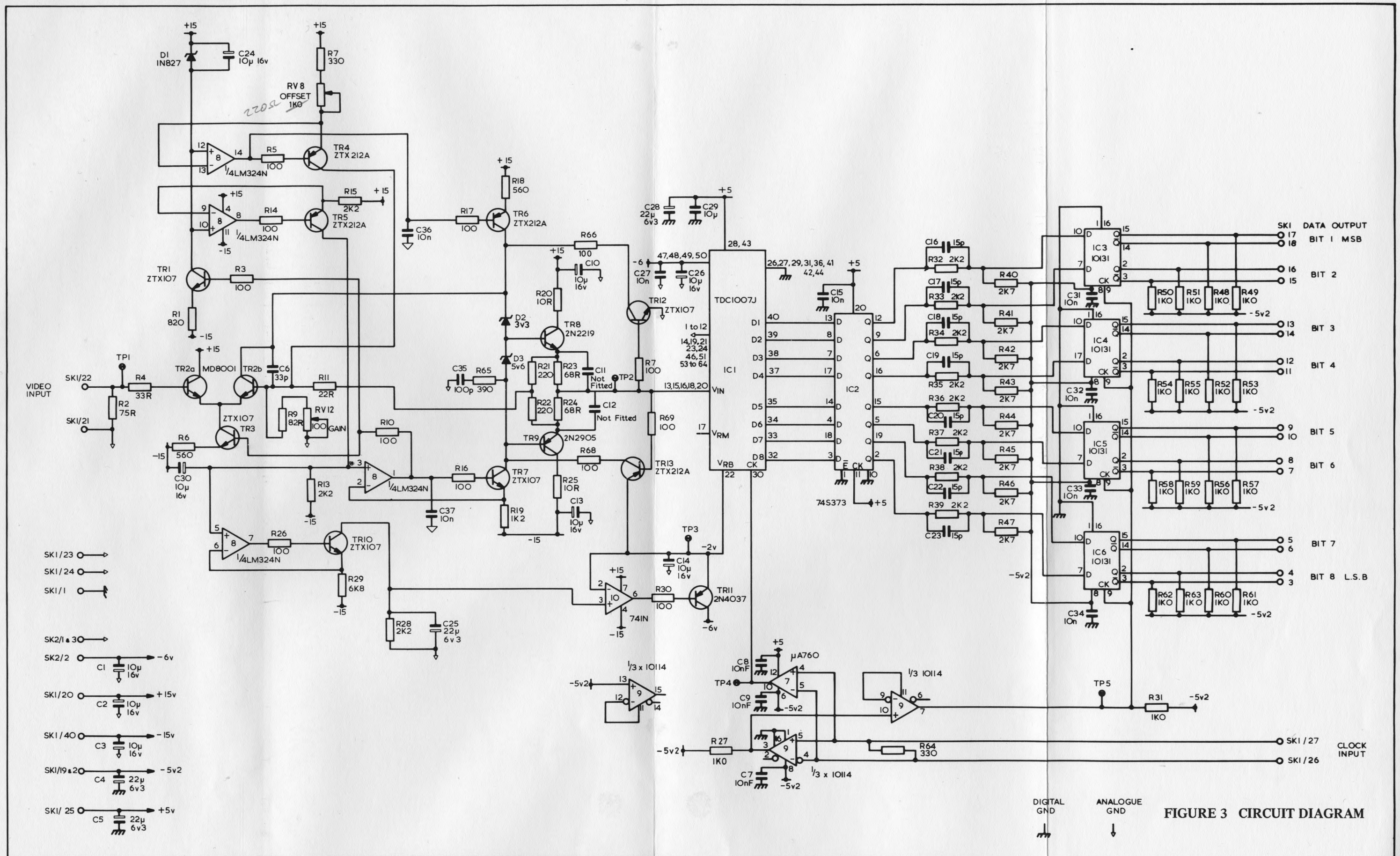


FIGURE 3 CIRCUIT DIAGRAM

4H/16H
STORE

4H STORE
IVC PCB GL202

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FIGURE 1	BLOCK DIAGRAM, VIDEO PATH
FIGURE 2	BLOCK DIAGRAM, V.T.R. SYNC GENERATOR
FIGURE 3	COMPONENT LAYOUT
FIGURE 4	CIRCUIT DIAGRAM

4H STORE

IVC PCB GL202

INTRODUCTION

The Store card contains the majority of the digital circuitry used in the signal path in the TBC-2002. The card also contains the 28.8MHz oscillator for the read and write clocks for the main store, with associated counters and phase detectors. Also located on the card is the circuitry for the VTR sync pulse generation.

CIRCUIT DESCRIPTION

Signal Path

The 8-bit balanced chroma and luminance data are connected in parallel to the Store card through twisted pair cables via SK5 and SK6 respectively. Each balanced bit is taken to a line receiver (IC1, 2, 3, 4) with tri-state outputs. IC1 and 2 receive the luminance data (YD1 – YD8) and the outputs are enabled by the Y MPX control signal, and IC3 and 4 receive chrominance data (CD1 – CD8) and are enabled by the CHROMA MPX control signal. These control signals enter the Store card at SK4/14 and 15 from the Input Oscillator card. In colour mode, the luminance and chrominance pairs of line receiver outputs are alternately enabled to multiplex chroma samples with luminance samples. In monochrome mode, IC1 and 2 are continuously enabled, IC3 and 4 are inhibited. In both colour and monochrome modes, the data rate at the multiplexer output is 14.4M words per second.

The output of the colour/luminance multiplexer is connected to a three-way demultiplexing circuit consisting of IC5, 6, 7, 10, 12, 14. The demultiplexing function is obtained by placing a 3-element shift register (IC5, 6, 12) in the path of each data bit so that a 24-bit word is available simultaneously at a 4.8M word/sec rate. This 24-bit word is latched by IC7, 10, 14, and passed

in parallel format to the inputs of the buffer store.

The buffer store is composed of six 4 x 4 register files (IC8, 9, 11, 13, 15, 16) so that it offers four storage locations for 24-bit words. The input address counter for the buffer store is IC17 and the output address counter is IC18. These two divide-by-four circuits are reset to a fixed count each line by the $\overline{\text{fH STOP}}$ signal from the Input Oscillator card via SK4/11. The reset pulse on IC18 is released two clock pulses after that on IC17, thus setting the buffer to the centre of its ± 2 clock pulse window at the start of each line.

The buffer store enables the write and read operations on the store card to be asynchronous, i.e. write and read clock pulses may occur at any relative phase and this phase may change continuously along a single line. This requirement is essential in a Time Base Corrector where the input clocks are locked to the "off tape" signal while the output clocks are locked to a stable reference.

The main store consists of 24 x 1024 bit random access memories (IC19 – IC42). Each cycle time of 4.8M words/sec (208ns) is separated into a WRITE and a READ cycle, each of 104ns, by the WE input to each RAM. A 10-bit address word is connected in parallel to all 24 RAMs. The two most significant bits of the address (A8, A9) provide the line address, while the lower eight bits provide the 256 samples within each active line. (Due to the three-way demultiplexing, there are in effect 768 samples per line).

The write and read addresses are alternately connected to the RAMs by means of address multiplexing circuits IC46, 51 and 52. These address multiplexers are enabled by a 4.8MHz square wave derived from the 28.8MHz oscillator. The 24-bit outputs of the RAMs are fed to D-type latches, IC43, 44, 45, whereby, by enabling the tri-state output of each in turn, the 24-bit word is remultiplexed to form an 8-bit word.

Clock Circuitry

14.4MHz TTL level clocks from the Input Oscillator card enter the Store card at SK4/16 and are used to clock the demultiplexer shift registers (IC5, 6 and 12) and a "ring of 3" circuit (IC71 and IC70/3) which provides the clocks for the demultiplexer latches (IC7, 10, 14).

The "off tape" horizontal pulse, $\overline{fH\ STOP}$, connected at SK4/11 is used to reset the "ring of 3" and is relatched against the output clocks in IC69. These horizontal pulses also reset the address counters for the buffer store (IC17 and 18).

The 28.8MHz (1848fH) oscillator which generates the READ and WRITE clocks to the main store is phase-locked to the READ H pulse from the Sync Pulse Generator card which enters the Store card at SK1/8. The pulse is delayed by monostable IC63 which allows adjustment of picture to sync timing. The output of IC63 is connected to one input of a phase comparator circuit (IC64). The other input to the phase comparator is from the output of the READ clock pulse counter for the main store.

The oscillator, which is voltage controlled by means of varactor diode D3, runs at a frequency of 1848 times horizontal frequency. The sinewave output is converted to TTL level by IC66. The output at IC58/3 (monitored at TP4) is taken from the Store card to the Output Processor card via SK3/8, and is also used to clock a divide-by-two counter (IC62/3) and a divide-by-six counter (IC61 and IC62/11). The 14.4MHz output of the divide-by-two counter (monitored at TP3) is taken to the Output Processor card via SK3/6, and also to a "ring of 3" circuit (IC59 and IC60/11) which provides the clocks for the remultiplexer latches. The square wave output of the divide-by-six counter drives both the READ clock counter and the WRITE clock counter as well as the write enable pulse generator and the address multiplexers.

The two most significant bits of the store address, i.e. the line address bits, are derived from the $\overline{FLYWHEEL\ fH}$ signal from the Input Oscillator card via SK4/12 and the READ H signal from the Sync Pulse Generator card via SK1/8, and are input to the store RAMs via address multiplexers IC46.

The READ clock counter consists of IC53, 54, 55, 56, and counts up from zero to a maximum of 307 (i.e. 308 pulses). The 8-bit output from IC53 and 54 form the lower eight bits of the READ address to the main store and are input via address multiplexers IC51. When the count of 307 is reached, it is decoded by IC55 which resets the counter to zero and causes a narrow RESET pulse

to be generated at IC57/6. This pulse resets the divide-by-two and divide-by-six counters and associated "ring of 3" circuit, and is taken to the Output Processor card via SK3/10.

The WRITE clock counter consists of IC67 and 68. The 8-bit output provides the lower eight bits of the WRITE address which are input to the main store via address multiplexers IC52.

The horizontal pulse, $\overline{fH\ STOP}$, clocks IC70/11 on each line via shift registers IC69 causing its Q output to go high. This allows write enable pulses WE from pulse generator IC72 to pass through to IC57/8 which drives all 24 RAMs in the main store. These pulses determine whether data is written into or read from the store. When the WRITE counter reaches full count (255) IC70/13 is cleared and inhibits any further WE pulses. This ensures there are only 256 WE pulses per line. These WE pulses may also be disabled by the DOC signal input from the Sync Pulse Generator card via SK1/16. IC95 is a retriggerable monostable driven by the horizontal pulse $\overline{fH\ STOP}$. When the input to the TBC-2002 is removed and the H pulses disappear, IC95 relaxes and the WE pulses are permanently enabled. This ensures that black level is written into the store and therefore the TBC output is at black level.

Read/Write Phasing Control

The write line address bits are generated by IC49, and the read line address bits by IC50. For optimum timebase correction window, it is necessary for the write sequence to be two lines in advance of the read sequence. This is monitored by IC48, which subtracts the write line address from the read line address. The $\Sigma 1$ and $\Sigma 2$ outputs from IC48 are taken to NAND gates IC47. For optimum conditions, $\Sigma 1$ is high and $\Sigma 2$ low so that IC47/8 is low.

The MATCH RESET pulse, connected to IC47 pins 1 and 2, is normally low (forcing IC47/12 high), but a narrow positive pulse occurs when the "off tape" field sync is exactly two lines in advance of the output field sync (which condition is indicated by IC76/13 going high). If the read/write phasing is correct when the MATCH RESET pulse occurs, IC47/12 remains high and no action is taken. If however, the phasing is incorrect (i.e. not two lines apart) IC47/12 goes low and resets IC49 and IC50 to a count which is two lines apart.

VTR Sync Generator Circuit

The VTR generator circuit provides a pseudo mixed sync signal for output to the VTR LOCK connector on the rear panel. It includes a control

loop which allows the VTR syncs to be advanced or retarded in order to maintain the mean write and read timing functions of the main store at two lines apart. It also contains a matching circuit which ensures that the TBC output sync and the VTR sync frame-match, which is necessary if a VTR capable of frame-locking is in use.

Programmable divider IC83 and IC84 form a divide-by-227 circuit clocked by 454fH pulses input on SK1/11 from the Sync Pulse Generator card. The output from the counter is at twice horizontal frequency (2fH) and clocks a divide-by-625 counter IC73. Decoder IC75/1 goes low at count 624, and at the next clock pulse the $\bar{Q}$ output on IC76/2 goes high resetting IC73 via the differentiator C28 and R53.

IC74 decodes a pulse of 8 clock pulse widths which is used to select horizontal sync pulses or broad pulses via a switching arrangement (IC78). The output from the switch on IC78/4 is the pseudo mixed sync signal whose field group consists of eight half line broad pulses. This pseudo mixed sync signal is connected to the Sync Pulse Generator card via SK1/9.

IC88/3 is clocked with twice horizontal frequency pulses and produces horizontal sync pulses via differentiator C35 and R51. The broad pulse serration width is determined by differentiator C24 and R50.

IC88/11 is clocked by a narrow pulse derived from pulses REF V and ODD/EVEN from the Sync Pulse Generator card (via SK1/10 and 15) once per frame. IC88/10 is reset by the VTR sync generator field pulse from IC76. The output pulse from IC88/13 is gated against the horizontal frequency square wave from IC88/1 and is used to reset the phase of the divide-by-two circuit at IC88/6 if the monochrome framing of the TBC output and VTR sync do not match.

In order that the mean write and read timing functions of the main store may be kept two lines apart, various vertical references are compared in order to change the divide ratio of IC83 and 84 as and when required. One vertical pulse is obtained from IC87/13 by latching the OFF TAPE V sync (which enters the card at SK4/13 from the Input Processor card) with the FLYWHEEL fH signal (which enters the card at SK4/12 from the Input Oscillator card). Another vertical pulse is derived from IC87/1 by latching the REF V pulse from the Sync Pulse Generator card (via SK1/10) with the READ H pulse (via SK1/8). These two related vertical pulses are applied to transmission gates IC85/8 and 1. The V BURST BLK input from the Sync Pulse Generator from SK1/13 is applied to IC85/4, and the $\bar{Q}$ output from IC93/9 is applied to IC85/11. With V PHASE AUTO selected on the

front panel, the control inputs to IC85 connect pins 8 to 9 and pins 1 to 2 thereby switching the two related vertical pulses through to phase comparator IC86.

Whichever vertical pulse occurs first clocks its half of IC86 and causes the $\bar{Q}$ output to go low thus sending IC90/11 high. After a delay determined by R35 and C15, this clocks IC89/11. If the other vertical pulse occurs within the period of a few microseconds (as set by R35 and C15), IC92/4 goes high and sets IC89/8 via D5. This ensures that no action is taken to change the count of the programmable divider (IC83 and 84).

If, however, the latter vertical pulse does not occur until after IC89/11 has been clocked, IC89/13 goes low and causes IC86/10 or IC86/4 to be held high. This holds both halves on IC86 static and the relative phase of the input vertical pulses is indicated by whichever $\bar{Q}$ output is low. This state is passed via IC92/3 and 11 to the program inputs of IC84 to either keep the count at 227 or change it to 225 or 229.

With the V PHASE AUTO control on the front panel in the OFF position, i.e. manual control of the VTR syncs is selected, the control inputs to IC85 connect pins 4 to 3 and pins 11 to 10. This connects the V BURST BLK reference signal and the output pulse from IC93/9 through to phase comparator IC86. The period of the pulse from IC93/9 controls the count on IC84 and is variable from the control on the front panel via operational amplifier IC79.

The number of lines in one field for which a count from IC84 remains changed is determined by the wire links on selector switches IC80 and IC81. There are two sets of links on each switch:—

$X_0 Y_0 Z_0$ determine the manual count change period.

$X_1 Y_1 Z_1$ determine the auto count period.

The outputs from IC80 and IC81 are fed to the inputs of a programmable shift register IC82. The input of this register (IC82/7) is permanently connected high, and it is clocked by the 2fH pulse from IC83/11.

When a vertical pulse clocks one half of IC86 and IC90/11 goes high, IC82/3 and IC89/4 are both reset so that IC82/10 and IC89/1 go low. Successive 2fH clock pulses on IC82/4 move highs from the input through the shift register. After a preset number determined by the programmed inputs, IC82/10 goes high and clocks IC89/3. This causes IC89/1 to go high and set IC89/8 which returns the count to 227.

For each frame, IC86 is reset to its initial condition of both $\bar{Q}$ outputs high by a pulse on IC91/6 and 8 which is derived from the REF V and ODD/EVEN inputs from the Sync Pulse Generator (SK1/10 and 15) via IC93/6 and IC65/4.

ADJUSTMENTS

RV1 – Adjusts the peak-to-peak amplitude of the 28.8MHz oscillator. This is monitored on IC66 pin 3, and is set at 1V.

RV2 – Provides horizontal phase adjustment of the output picture. It is adjusted in monochrome mode only to give correct picture timing with respect to synchronous pulses whilst observing the output signal.

L1 – Sets the 28.8MHz oscillator control volts. It is adjusted to give 2.5V monitored on TP11.

CONNECTIONS

SK1 Sync Pulse Generator Card Connections

8	READ H
9	$\overline{\text{VTR SYNC}}$
10	REF V
11	454fH
12	OFF TAPE V
13	V BURST BLK
14	REF V
15	ODD/EVEN
16	$\overline{\text{DOC}}$

SK2 Power Connections

2	-15V
3	Ground
4,5,6	+5V
7,8,10	Ground
11,12	-5.2V
13,14	Ground
15	+15V

SK3 Output Processor Card Connections

1	Bit 8	} Output picture data
2	Bit 1	
3	Bit 7	
4	Bit 2	
6	14.4MHz CKS	
8	28.9MHz CKS	
10	RESET	

12	Bit 4	} Output picture data
13	Bit 5	
14	Bit 3	
15	Bit 6	

SK4 Input Circuitry Control Signals

6	OV (AUTO/ $\overline{\text{MANUAL}}$)
7	+15V (V PHASE CONTROL)
8	V PHASE CONTROL
9	OV (V PHASE CONTROL)
10	AUTO/ $\overline{\text{MANUAL}}$
11	fH STOP
12	$\overline{\text{FLYWHEEL fH}}$
13	OFF TAPE V
14	Y MPX
15	CHROMA MPX
16	14.4MHz CKS TTL

SK5 Chrominance Digital Data Input

1	Bit 1 (MSB)
2	Bit 2
3	Bit 3
4	Bit 4
5	Bit 5
6	Bit 6
7	Bit 7
8	Bit 8
9	Bit 8 (LSB)
10	Bit 7
11	Bit 6
12	Bit 5
13	Bit 4
14	Bit 3
15	Bit 2
16	Bit 1

SK6 Luminance Digital Data Input

1	Bit 1 (MSB)
2	Bit 2
3	Bit 3
4	Bit 4
5	Bit 5
6	Bit 6
7	Bit 7
8	Bit 8
9	Bit 8
10	Bit 7
11	Bit 6
12	Bit 5
13	Bit 4
14	Bit 3
15	Bit 2
16	Bit 1

TEST POINTS

TP1 Earth
 TP2 RESET Pulse
 TP3 14.4Mpz clocks, output
 TP4 28.9MHz clocks
 TP5 Drop-out pulse
 TP6 14.4MHz clocks, input
 TP7 fH STOP signal
 TP8 Address multiplex data

TP9 Earth
 TP10 Earth
 TP11 Oscillator control volts
 TP12 FLYWHEEL fH signal
 TP13 Phase shifted READ H signal
 TP14 Store phasing signal
 TP15 VTR SYNC field pulse
 TP16 Earth

CIRCUIT REF.	DESCRIPTION	PART NO.
	CAPACITORS	
C1	120pF $\pm 2\frac{1}{2}\%$, 63V	R511215
C2	10nF, 25V	R501033
C3	47pF $\pm 2\frac{1}{2}\%$, 63V	R514705
C4	1000pF, 63V	R511025
C5	10nF $\pm 10\%$, 100V	R521036
C6	100nF $\pm 10\%$, 100V	R521046
C7	100pF $\pm 2\frac{1}{2}\%$, 63V	R511015
C8	22pF $\pm 2\frac{1}{2}\%$, 63V	R512205
C9	22pF $\pm 2\frac{1}{2}\%$, 63V	R512205
C10	10nF, 25V	R501033
C11	10nF, 25V	R501033
C12	10nF, 25V	R501033
C13	10nF, 25V	R501033
C14	10nF, 25V	R501033
C15	1000pF $\pm 2\frac{1}{2}\%$, 63V	R511025
C16	4700pF, 63V	R514725
C17	330pF $\pm 2\frac{1}{2}\%$, 63V	R513325
C18	100pF $\pm 2\frac{1}{2}\%$, 63V	R511015
C19	560pF, 63V	R515615
C20	10nF, 25V	R501033
C21	10nF, 25V	R501033
C22	680pF $\pm 2\frac{1}{2}\%$, 63V	R516815
C23	330pF $\pm 2\frac{1}{2}\%$, 63V	R513315
C24	220pF $\pm 2\frac{1}{2}\%$, 63V	R512215
C25	220pF $\pm 2\frac{1}{2}\%$, 63V	R512215
C26	220pF $\pm 2\frac{1}{2}\%$, 63V	R512215
C27	220pF $\pm 2\frac{1}{2}\%$, 63V	R512215
C28	220pF $\pm 2\frac{1}{2}\%$, 63V	R512215
C29	10 μ F, 16V	R541062
C30	220pF $\pm 2\frac{1}{2}\%$, 63V	R512215
C31	10 μ F, 16V	R541062
C32	10 μ F, 16V	R541062
C33	22 μ F, 6.3V	R542261
C34	22 μ F, 6.3V	R542261

CIRCUIT REF.	DESCRIPTION	PART NO.
	CAPACITORS (continued)	
C35	150pF $\pm 2\frac{1}{2}\%$, 63V	R511515
C36	1000pF, 25V	R501023
C37	220pF, 63V	R502215
C38	100nF $\pm 10\%$, 100V	R521046
C39	Not fitted	—
C40 – C105	10nF, 25V	R501033
C106	10nF $\pm 10\%$, 100V	R521036
C107	10nF, 25V	R501033
C108	Not fitted	—
CV1	2-22pF, variable	R591222
CV2	Not fitted	—
	DIODES	
D1	1N4148	R354148
D2	1N4148	R354148
D3	BA102B	R372102
D4	1N4148	R354148
D5	1N4148	R354148
D6	1N4148	R354148
	INTEGRATED CIRCUITS	
IC1	MC3431	R283431
IC2	MC3431	R283431
IC3	MC3431	R283431
IC4	MC3431	R283431
IC5	74LS374	R240374
IC6	74LS374	R240374
IC7	74LS374	R240374
IC8	74LS670	R240670
IC9	74LS670	R240670
IC10	74LS374	R240374
IC11	74LS670	R240670
IC12	74LS374	R240374
IC13	74LS670	R240670
IC14	74LS374	R240374
IC15	74LS670	R240670

CIRCUIT REF.	DESCRIPTION	PART NO.
INTEGRATED CIRCUITS (continued)		
IC16	74LS670	R240670
IC17	74LS74	R240074
IC18	74LS74	R240074
IC19 – IC42	P2125	R272125
IC43	74LS374	R240374
IC44	74LS374	R240374
IC45	74LS374	R240374
IC46	74S241	R230241
IC47	74LS10	R240010
IC48	74LS283	R240283
IC49	74LS74	R240074
IC50	74LS74	R240074
IC51	74S241	R230241
IC52	74S241	R230241
IC53	74S163	R230163
IC54	74S163	R230163
IC55	74S30	R230030
IC56	74S112	R230112
IC57	74S140	R230140
IC58	74S00	R230000
IC59	74S74	R230074
IC60	74S74	R230074
IC61	74S74	R230074
IC62	74S74	R230074
IC63	4098	R261098
IC64	4013B	R261013
IC65	4001B	R261001
IC66	NE529N	R280529
IC67	74LS161	R240161
IC68	74LS161	R240161
IC69	74LS174	R240174
IC70	74S74	R230074
IC71	74S74	R230074
IC72	74122	R210122

CIRCUIT REF.	DESCRIPTION	PART NO.
INTEGRATED CIRCUITS (continued)		
IC73	4040B	R261040
IC74	4078B	R261078
IC75	4012B	R261012
IC76	4013B	R261013
IC77	4069B	R261069
IC78	4011B	R261011
IC79	74145	R210145
IC80	4053B	R261053
IC81	4053B	R261053
IC82	14557B	R261557
IC83	74LS161	R240161
IC84	74LS161	R240161
IC85	4066B	R261066
IC86	4013B	R261013
IC87	4013B	R261013
IC88	4013B	R261013
IC89	4013B	R261013
IC90	4011B	R261011
IC91	4001B	R261001
IC92	4001B	R261001
IC93	4098	R261098
IC94	4098	R261098
IC95	74LS122	R240122
INDUCTORS		
L1	Type AH	R600233
L2	22 μ H	R620223
RESISTORS		
R1 – R16	330 $\pm$ 5%, $\frac{1}{3}$ W	R401334
R17	10k $\pm$ 5%, $\frac{1}{3}$ W	R401106
R18	1k0 $\pm$ 5%, $\frac{1}{3}$ W	R401105
R19	1k5 $\pm$ 5%, $\frac{1}{3}$ W	R401155
R20	220 $\pm$ 5%, $\frac{1}{3}$ W	R401224
R21	100 $\pm$ 5%, $\frac{1}{3}$ W	R401104
R22	5k6 $\pm$ 5%, $\frac{1}{3}$ W	R401565

CIRCUIT REF.	DESCRIPTION	PART NO.
	RESISTORS (continued)	
R23	47k $\pm$ 5%, $\frac{1}{3}$ W	R401476
R24	1k0 $\pm$ 5%, $\frac{1}{3}$ W	R401105
R25	10k $\pm$ 5%, $\frac{1}{3}$ W	R401106
R26	10k $\pm$ 5%, $\frac{1}{3}$ W	R401106
R27	15k $\pm$ 5%, $\frac{1}{3}$ W	R401156
R28	100k $\pm$ 5%, $\frac{1}{3}$ W	R401107
R29	470 $\pm$ 5%, $\frac{1}{3}$ W	R401474
R30	47k $\pm$ 5%, $\frac{1}{3}$ W	R401476
R31	10k $\pm$ 5%, $\frac{1}{3}$ W	R401106
R32	10k $\pm$ 5%, $\frac{1}{3}$ W	R401106
R33	1k0 $\pm$ 5%, $\frac{1}{3}$ W	R401105
R34	1k0 $\pm$ 5%, $\frac{1}{3}$ W	R401105
R35	4k7 $\pm$ 5%, $\frac{1}{3}$ W	R401475
R36	22k $\pm$ 5%, $\frac{1}{3}$ W	R401226
R37	4M7 $\pm$ 10%, $\frac{1}{3}$ W	R401478
R38	3k3 $\pm$ 5%, $\frac{1}{3}$ W	R401335
R39	27k $\pm$ 5%, $\frac{1}{3}$ W	R401276
R40	47k $\pm$ 5%, $\frac{1}{3}$ W	R401476
R41	47k $\pm$ 5%, $\frac{1}{3}$ W	R401476
R42	1k0 $\pm$ 5%, $\frac{1}{3}$ W	R401105
R43	470 $\pm$ 5%, $\frac{1}{3}$ W	R401474
R44	470 $\pm$ 5%, $\frac{1}{3}$ W	R401474
R45	1M0 $\pm$ 10%, $\frac{1}{3}$ W	R401108
R46	47k $\pm$ 5%, $\frac{1}{3}$ W	R401476
R47	47k $\pm$ 5%, $\frac{1}{3}$ W	R401476
R48	1k0 $\pm$ 5%, $\frac{1}{3}$ W	R401105
R49	10k $\pm$ 5%, $\frac{1}{3}$ W	R401106
R50	47k $\pm$ 5%, $\frac{1}{3}$ W	R401476
R51	47k $\pm$ 5%, $\frac{1}{3}$ W	R401076
R52	47k $\pm$ 5%, $\frac{1}{3}$ W	R401476
R53	47k $\pm$ 5%, $\frac{1}{3}$ W	R401476
R54	47k $\pm$ 5%, $\frac{1}{3}$ W	R401476
R55	22k $\pm$ 5%, $\frac{1}{3}$ W	R401226
R56	47k $\pm$ 5%, $\frac{1}{3}$ W	R401476

CIRCUIT REF.	DESCRIPTION	PART NO.
	RESISTORS (continued)	
R57	10k $\pm 5\%$, $\frac{1}{3}$ W	R401106
R58	820k $\pm 5\%$, $\frac{1}{3}$ W	R401827
R59	47k $\pm 5\%$, $\frac{1}{3}$ W	R401476
R60 – R65	Not fitted	—
R66	4M7 $\pm 10\%$, $\frac{1}{3}$ W	R401478
R67	47k $\pm 5\%$, $\frac{1}{3}$ W	R401476
RV1	4k7, variable	R492475
RV2	10k, variable	R492106
	CONNECTORS	
SK1	Socket, 16-pin DIL	R808016
SK2	2-part connector, 16-way	R810116
SK3	Socket, 16-pin DIL	R808016
SK4	Socket, 16-pin DIL	R808016
SK5	Socket, 16-pin DIL	R808016
SK6	Socket, 16-pin DIL	R808016
	TRANSISTORS	
TR1	E300	R320300
TR2	ZTX212AL	R348212

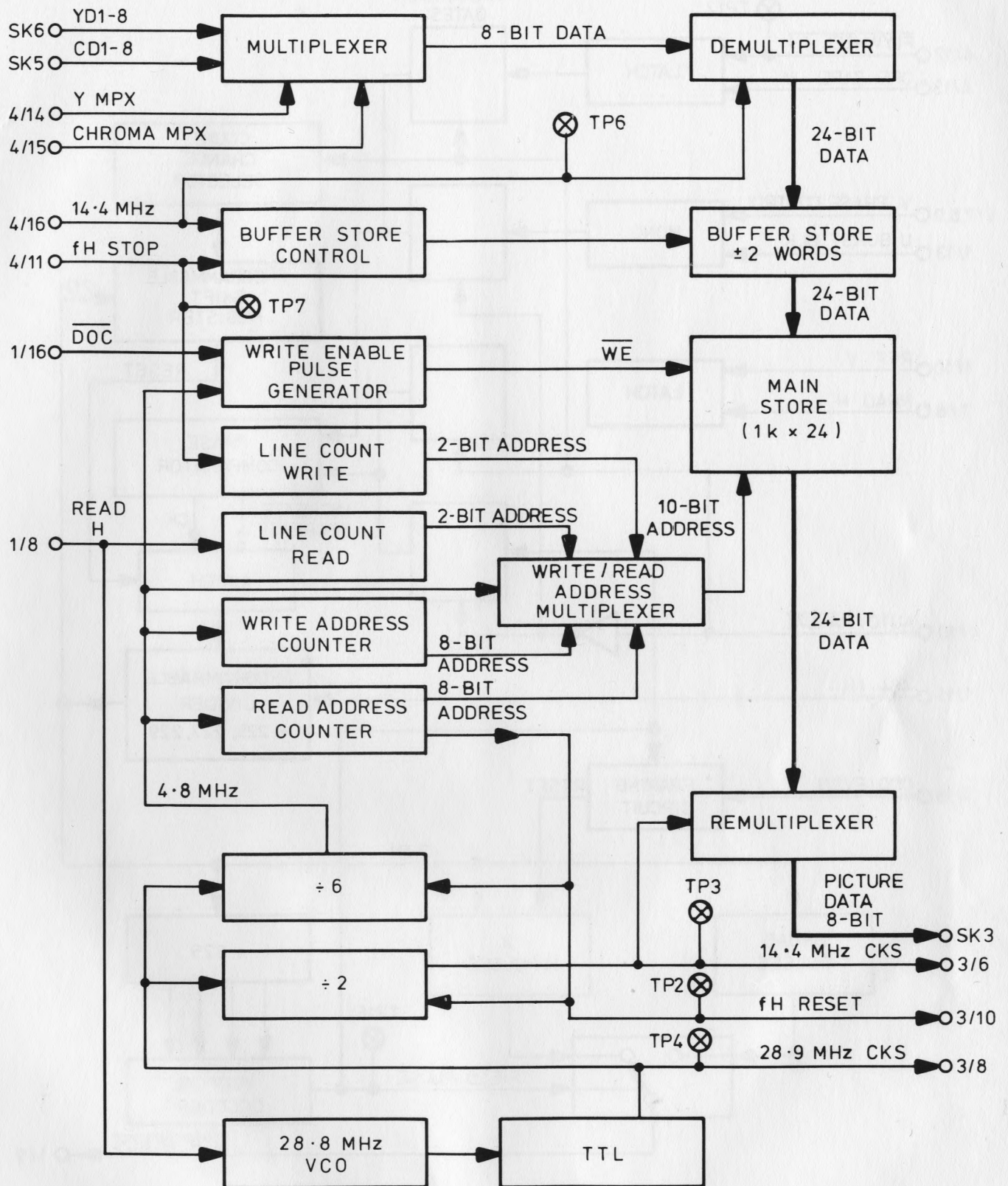


FIGURE 1 BLOCK DIAGRAM, VIDEO PATH

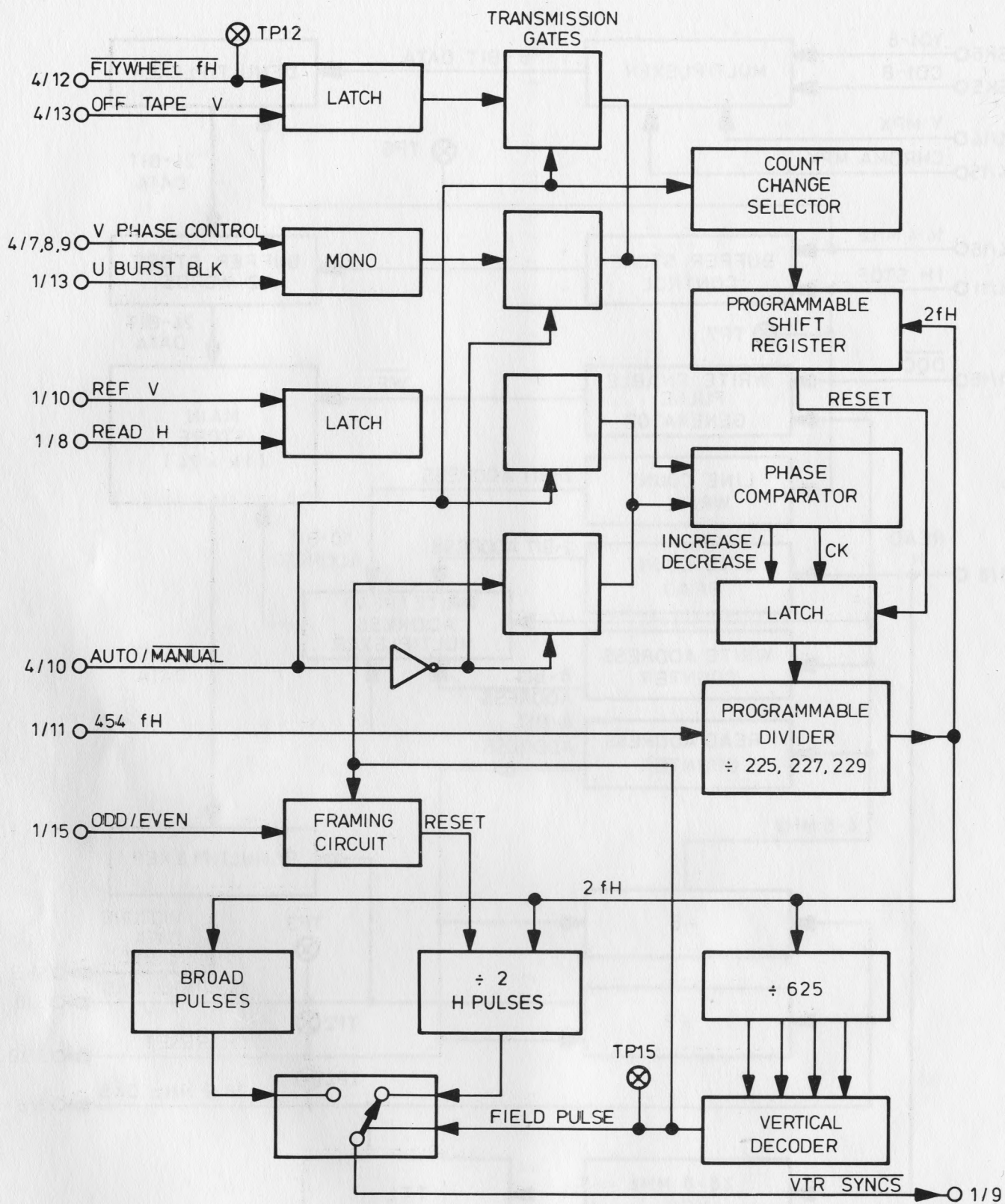


FIGURE 2 BLOCK DIAGRAM, V.T.R. SYNC GENERATOR

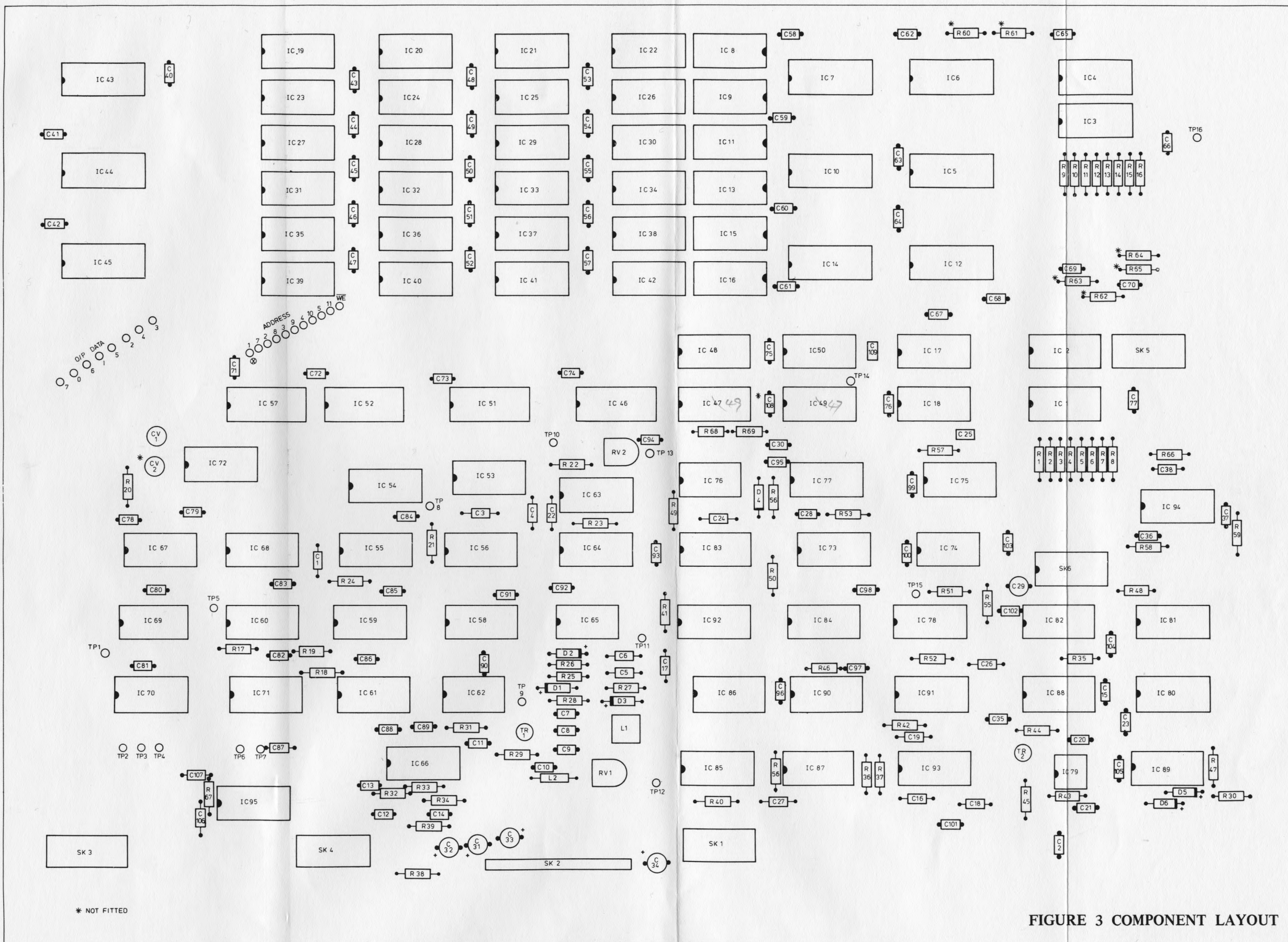


FIGURE 3 COMPONENT LAYOUT

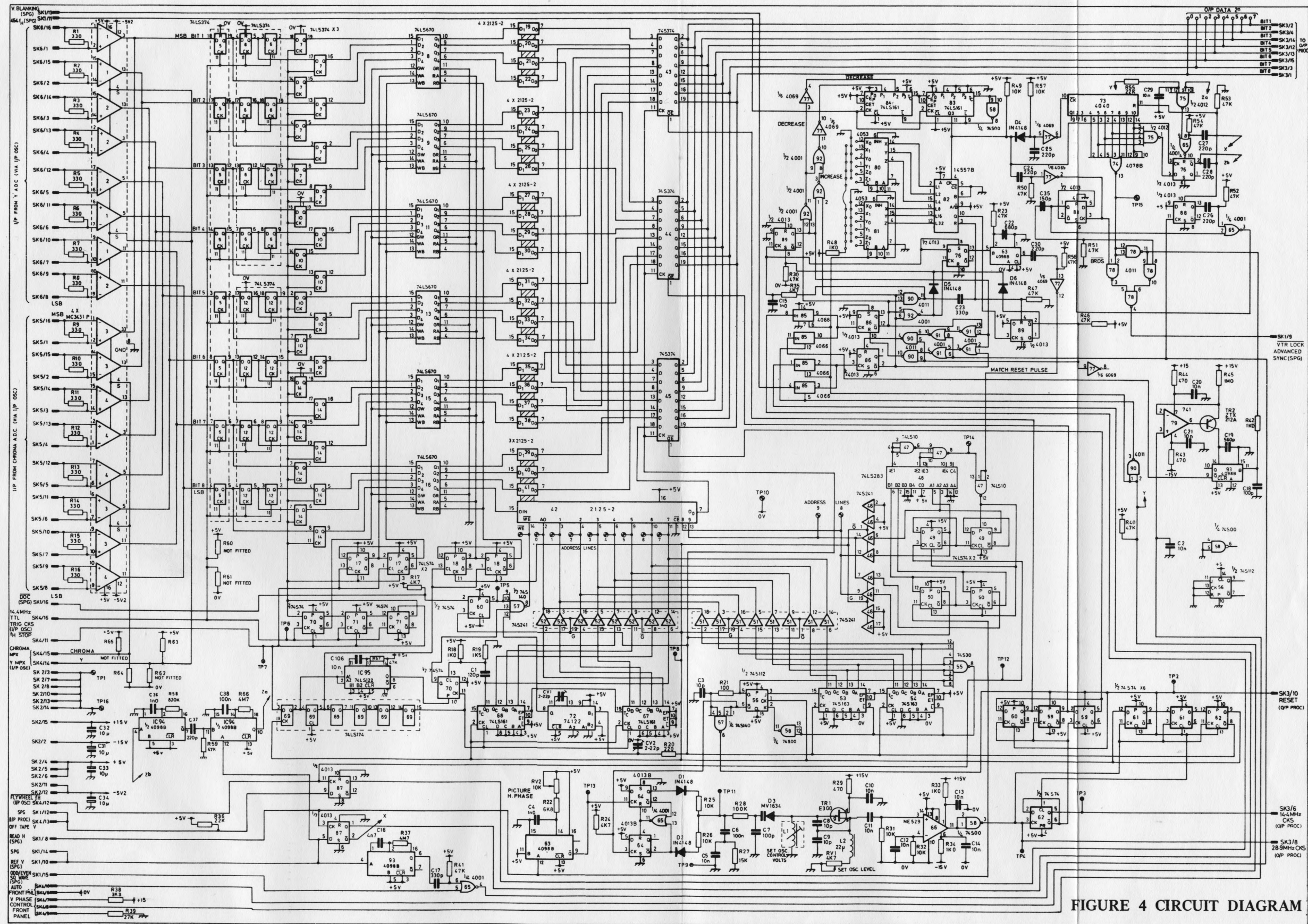


FIGURE 4 CIRCUIT DIAGRAM

16H STORE CARD
IVC PCB GL215

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CIRCUIT DESCRIPTION	1

FIGURE 1	COMPONENT LAYOUT
FIGURE 2	CIRCUIT DIAGRAM

16H STORE CARD

IVC PCB GL215

INTRODUCTION

The 16H Store card is similar in operation to the 4H Store card (GL202). It employs 4k static random access memories in place of the 1k devices used on the 4H Store card, and therefore, there are 12 address lines on the 16H Store card. Other differences between the cards lie in the area of the write and read line address counters.

CIRCUIT DESCRIPTION

The following notes outlining the differences on the 16H Store card should be read in conjunction with the circuit description for the 4H Store card.

The write address counter consists of half IC49 (74LS393) which is a dual 4-bit counter. It is clocked by the flywheel fH signal on IC49/1. The four most significant write addresses (8, 9, 10,

11) on IC49/3, 4, 5, 6 are fed via tri-state buffers (IC46) to the RAM address lines.

The read address counter is the other half of IC49 and is clocked by the READ H signal on IC49/13. The four outputs are also fed via tri-state buffers IC46 to the RAM address lines.

IC46 is the WRITE/READ address multiplexer and is controlled by the 4.8MHz square wave on pins 1 and 19.

IC48 is connected to subtract the value of the read address from the write address. It is required that the average difference between the write and read address is 8 lines. When a "field pulse match" pulse occurs, the write and read address counters are reset via IC49 pins 2 and 12 to a relative phase difference of 8 lines.

In order to achieve the average 8H advance of the input relative to the output required by the 16H Store card, the type V2 PROM (IC7) on the Sync Pulse Generator card (GL207) is replaced by a type V3 PROM.

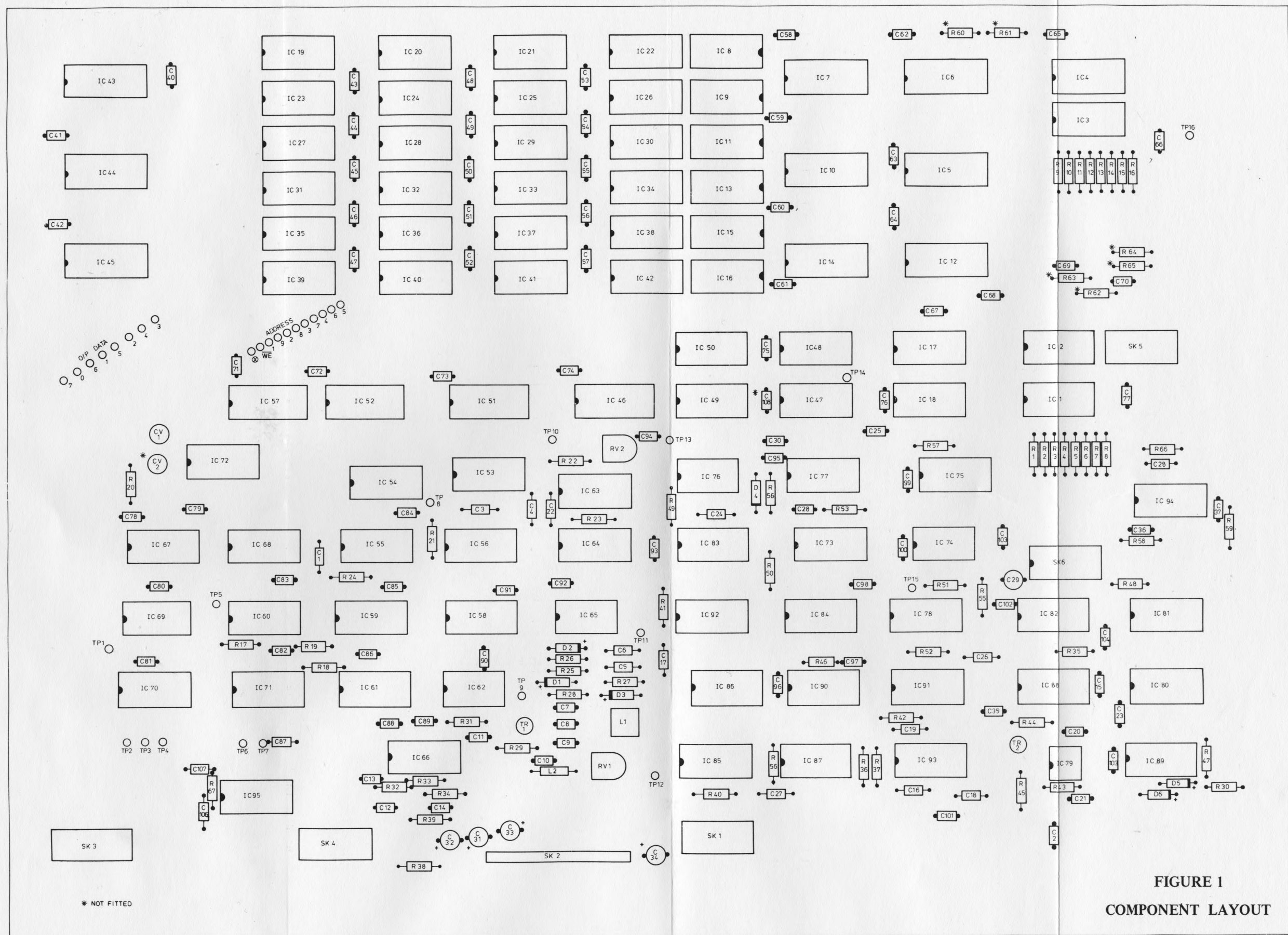
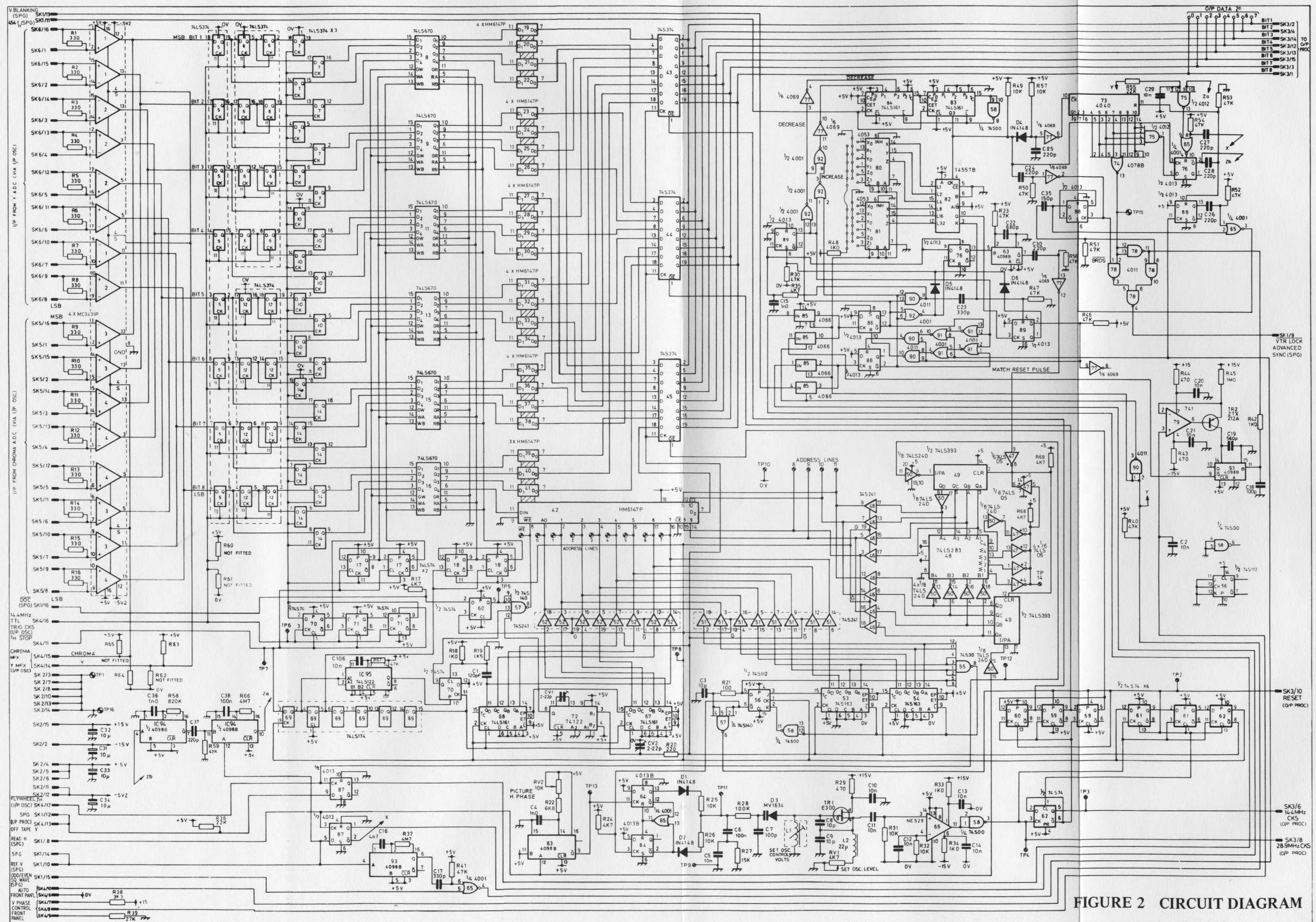


FIGURE 1
COMPONENT LAYOUT



OUTPUT
PROCESSOR

OUTPUT PROCESSOR
IVC PCB GL205

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CIRCUIT DESCRIPTION	1
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COMPONENT SCHEDULE	5

FIGURE 1	BLOCK DIAGRAM
FIGURE 2	COMPONENT LAYOUT
FIGURE 3	CIRCUIT DIAGRAM

OUTPUT PROCESSOR

IVC PCB GL205

INTRODUCTION

The Output Processor card GL205 contains the circuitry for reconstituting the composite video signal from the digital picture data.

The picture data is first separated into the luminance and chrominance components and these are converted into analogue format by three separate digital-to-analogue converters (DACs). After processing, these signals are added to syncs to form a composite PAL colour signal which is buffered and output to the rear panel connectors.

The card also contains two relays: The BYPASS relay, and the COLOUR/MONO relay which routes the luminance signal through the appropriate filter on the Output Filter card.

CIRCUIT DESCRIPTION

Luminance/Chrominance Separation

8-bit picture data from the Store card is input to the Output Processor card via SK1 and taken to latches IC1 and IC2. It is clocked through the latches by 14.4MHz clocks from the Store card via SK1/6 and IC11/2. (These clocks are precisely retimed in IC11/2 by the 28.9MHz clocks from the Store card on SK1/8. The outputs from latches IC1 and IC2 are connected to three demultiplexing octal latches, IC3, IC5, IC6. To separate the picture data into its luminance and chrominance components, it is necessary to clock the demultiplexing latches in sympathy with the pattern of the multiplexed input data (i.e. Y, R-Y, Y, B-Y sequence).

A 4-stage ring counter, IC14, IC15 provides four phases at 3.6MHz for clocking the demultiplexing latches such that IC3 outputs the luminance signal; IC5 the colour difference R-Y signal, and IC6 the colour difference B-Y signal. The ring

counter sequence is established by the horizontal RESET pulse from the Store card (SK1/10) to correctly demultiplex the picture data pattern. The clock for ring counter IC14, IC15 is the 14.4MHz clock from the Store card.

In colour mode, the MONO + NSS control (SK5/13) from the Input Processor is high and enables the outputs from the 4-phase counter to provide the necessary clocks. Phase 1 and 3 outputs (IC14/5 and IC15/5) are combined through IC12/11, 12, 13 to provide 7.2MHz clocks at IC12/8. These clocks are latched back against the 28.9MHz Store clocks at IC11/7 and provide the 7.2MHz luminance clocks for IC3. Phase 2 output (IC14/9) is enabled through IC13/11 and provides the 3.6MHz clocks for IC6 at IC11/11. Phase 4 output (IC15/9) is enabled through IC13/8 and provides the 3.6MHz clocks for IC5 at IC11/15.

In monochrome mode, gates IC13/8 and 11 are inhibited by the MONO + NSS signal so that the R-Y and B-Y demultiplexing latch clocks are inhibited. The 14.4MHz Store clocks are IC12/6 are enabled through to IC12/8 and provide 14.4MHz clocks for the luminance demultiplexing latch, IC3.

The colour difference outputs from IC5 and IC6 are taken direct to DACs IC9 and 10. The luminance output from IC3 is inverted and converted to ECL level by IC7, IC8 and relatched by IC17, IC18. These latches are also clocked from the 4-phase ring counter via IC11/7 and their outputs are applied to the luminance DAC IC16.

To establish a mid-range clamping reference in the chrominance paths (i.e. zero chrominance) during the H blanking period, the complement of picture data MSB (IC1/3) is inverted at IC4/8 and input as the MSB of each multiplexer latch IC5 and IC6. During the narrow blanking period the H pulse at SK2/4 clears latches IC1 and IC2 so that all Q outputs are low, and forces IC4/8 high. This sets

the MSB to latches IC5, IC6 high and other bits low so that the analogue output from the DACs IC9, IC10 is forced to mid-range.

In the luminance path, the low outputs from IC1, IC2 during the narrow blanking period are latched by IC3 and IC17, 18 to generate an output from DAC IC16 which corresponds to digital zero (i.e. black level).

Luminance Path

The analogue output from IC16/15 is a current output and is input to blanking modulator IC25 at pin 3. The blanking input on IC25/10 is derived from the BLANKING signal input from the Sync Pulse Generator card via SK2/13, and a reference potential is present at IC25/8. RV14 adjusts the pulse width of the blanking input. IC25 multiplies the analogue luminance signal by the blanking input, and RV16 sets the level of black clipping. The output on IC25/6 is again in current form and is passed through a virtual earth amplifier (TR32, TR34, TR11, TR33, TR35) to provide a voltage output of blanked luminance. This is monitored by TP13 and drives through 75 ohms to the Output Filter card via SK6/4 (for colour mode) or SK6/2 (for monochrome mode) as selected by relay RL2 (which is energised in the monochrome mode).

In monochrome mode, the luminance signal is limited to 5.5MHz on the Output Filter card and re-enters the Output Processor card via SK5/4. In colour mode, the luminance signal is band limited to 3MHz on the Output Filter card and passes via the Enhancer card before re-entering the Output Processor card on SK4/2 for syncs and chroma to be added.

Chrominance Paths

The R-Y and B-Y current outputs from DACs IC9 and IC10 are fed to virtual earth amplifiers comprising TR1, TR2, TR3, TR4 and TR12, TR13, TR5, TR14 which provide low impedance voltage outputs monitored at TP6 and TP7.

To remove glitches present at the DAC outputs, the chroma signals are resampled by diode ring switches D11-D14 and D16-D19. Balanced drives to these switches are derived from the phase 2 and phase 4 3.6MHz outputs of the ring counter via IC11/15, 14 and IC11/10, 11.

The sampled chroma signals are stored in C60 and C116 and buffered by FETs TR15 and TR16. The FET outputs are fed to chroma blanking demodulators IC19/4 and IC20/4 respectively, where they are multiplied by a blanking input derived from the BLANKING pulse at SK2/13 with timing adjusted by RV15.

The narrow blanking (H-pulse) from the Sync

Pulse generator card at SK2/4 is amplified by TR27 and drives FET analogue switches IC29/6 and IC29/5 to sample the mid-range operating voltage at IC19/3 and IC20/3 during blanking. This voltage is maintained by Op. Amps IC20 and IC31 during active picture time to provide the correct operating potential for gain setting resistors R83 and R161. At the output of the modulators, a burst flag is added to each colour difference signal.

The BURST GATE pulse from the Sync Pulse Generator card is input at SK2/14 to limiting amplifier TR17, TR18. It is filtered (C39, L7, C41) to provide a pulse with a controlled rise and fall time (monitored at TP8) and connected to the base of TR22 and TR36. These transistors add a burst flag current to the outputs from the blanking modulators (IC19/12, IC20/12) which may be adjusted by RV4 and RV5 to establish the correct R-Y and B-Y burst components respectively.

The current outputs from IC19/12 and IC20/12 are passed through virtual earth amplifiers (TR19, TR20, TR9, TR21 and TR23, TR24, TR10, TR25) and the resultant voltage signals may be monitored at TP9 and TP10. Each colour difference signal is fed through a 1.5MHz low pass filter which removes out-of-band components, and is input to a quadrature modulator (IC23, IC24). Balance controls RV7 and RV8 provide fine control of dc levels, to set R-Y and B-Y carrier balance.

Narrow blanking pulses, via TR27, sample the mid-range voltages at TP9 and TP10 with analogue switches IC29/12 and IC29/13 to maintain the correct modulator reference potentials at IC23/1 and IC24/5.

The 4.43MHz SUBCARRIER signal from the Sync Pulse Generator card (SK2/1) is input to IC21 and IC22. Network R115, C47 introduces a 45° phase lag into IC22, which acts as an amplitude limiter and the output from pin 12 is applied to B-Y modulator IC24/10. Network C43, R105, RV3 introduces a 45° phase lead into IC21 which acts as an amplitude limiter and phase splitter. RV3 sets 90° relationship between B-Y and R-Y subcarrier drives. The complementary outputs from IC21/6 and 12 are coupled via transformer T3 so that either phase of R-Y subcarrier drive is selected as determined by the polarity of the 7.8MHz IDENT signal from SK2/3 on IC21/4. The alternating phase output is coupled by T3 to the R-Y modulator IC23/10.

The outputs from IC23/12 and IC24/12 are coupled via test links 2 and 3 to a low pass filter (C90, L9, L10, C89) which removes unwanted harmonics before the combined chroma signal passes to the chrominance amplifier TR36, TR37, TR38. It is then fed through delay lines DL1 and DL2 to the chroma summing transistor TR39 which feeds it to the base of TR34.

Sync Separator

The COMPOSITE SYNC signal from the Sync Pulse Generator card (SK2/2) is gated through IC26 which selects delayed syncs in colour mode or undelayed composite syncs in monochrome mode. The delay circuit for colour comprises R205, RV11, C96, with RV11 providing adjustment of the timing of the output syncs. The selected syncs are applied to limiting amplifier TR40, TR41, with RV10 controlling the amplitude of the syncs to be added to the composite video. The low pass filter L8, C98, C100, C101 controls the rise and fall times of the syncs.

Composite Video Output Stage

The filtered luminance from contact RL2B, chrominance from the collector of TR39 and syncs from the collector of TR42 are summed at the base of TR43 and buffered by video amplifier TR43-TR48 inclusive. The main composite video output is switched to SK5/5 by bypass relay RL1, and taken to the BNC connector on the rear panel. The auxiliary video output is taken to the rear panel connector via SK5/11.

Bypass Mode

With BYPASS selected on the front panel, the PLAYBACK signal at SK5/7 is high and relay RL1 de-energised. Contacts of RL1B connect the BYPASS input on SK5/9 to the main video output at SK5/5. Similarly, if BYPASS is not selected but a power failure occurs, relay RL1 de-energises and connects the BYPASS video to the main video output.

ADJUSTMENTS

- RV3 – Adjusts quadrature of chrominance modulators.
- RV4 – Adjusts amplitude of R-Y component of burst.
- RV5 – Adjusts amplitude of B-Y component of burst.
- RV6 – Adjusts symmetry of swinging R-Y subcarrier fed to R-Y modulator.
- RV7 – Adjusts balance of R-Y modulator during blanking period. Adjust for zero subcarrier on sync bottoms.
- RV8 – Adjusts balance of B-Y modulator during blanking period. Adjust for zero subcarrier on sync bottoms.

RV9 – Adjusts amplitude of B-Y chrominance. Adjusts for correct ratio of B-Y to R-Y chrominance.

RV10 – Adjusts sync pulse amplitude.

RV11 – Adjusts output sync pulse timing to be the same with respect to picture information between colour and monochrome operation.

RV13 – Adjusts D.C. level of luminance signal. Adjusts for blanking level of 0V at TP13.

RV14 – Adjust timing of luminance blanking.

RV15 – Adjusts timing of chrominance blanking.

RV16 – Adjusts blanking level such that A.D.C. clips at a level below blanking.

LK1 – Places burst on O/P in monochrome mode. B to C, burst on. B to A, normal.

CONNECTIONS

SK1	Store card connections	
1	Bit 8 (LSB)	Picture data
2	Bit 1 (MSB)	
3	Bit 7	
4	Bit 2	
6	14.4MHz CKS	
8	28.9MHz CKS	
10	RESET	
12	Bit 4	Picture data
13	Bit 5	
14	Bit 3	
15	Bit 6	

SK2 Sync Pulse Generator card connections

1	SUBCARRIER
2	COMP SYNC
3	IDENT
4	H pulse
13	BLANKING
14	BURST GATE
15, 16	Ground (SUBCARRIER)

SK3 Power connections

2	+15V
3	0V
4,5,6	+5V
7,8	0V

SK3 Power connections (continued)

10	0V
11,12	-5.2V
13,14	0V
15	-15V

SK4 Enhancer card connections

1	LUM
2	Picture enhance CONTROL
3	CLAMP trigger
4	+5V
5	-5.2V
6	-15V
7	+15V
8	0V
9	Picture enhance ON/OFF
10	Picture enhance MAX
12	Picture enhance MIN
15,16	Ground (VIDEO)

SK5 Control and Video connections

1	Picture enhance MAX
2	Picture enhance CONTROL
3	Picture enhance MIN
4	Filtered luminance (MONO)
5	MAIN VIDEO output
6	Ground
7	PLAYBACK
8	Ground, filtered luminance
9	BYPASS VIDEO
10	Ground
11	AUX VIDEO
12	Ground
13	MONO + NSS

SK6 Output Filter card and Enhancer Switch Connections

1	0V
2	Luminance (MONO)
3	0V
4	Luminance (COLOUR)
5	Picture enhance ON/OFF

TEST POINTS

TP1	RESET pulse input
TP2	14.4MHz clocks
TP3	28.9MHz clocks
TP4	Sampled R-Y chroma
TP5	Sampled B-Y chroma
TP6	R-Y buffered DAC output
TP7	B-Y buffered DAC output
TP8	BURST GATE

TP9	R-Y with burst flag
TP10	B-Y with burst flag
TP11	R-Y input to modulator
TP12	B-Y input to modulator
TP13	Blanked luminance output
TP14	H pulse
TP15	Composite video signal at input to buffer amplifier

TP16,TP17 TP18,TP19	Ground
------------------------	--------

CIRCUIT REF.	DESCRIPTION	PART NO.
	CAPACITORS	
C1	10 μ F, 16V	R541062
C2	22 μ F, 6.3V	R542261
C3	22 μ F, 6.3V	R542261
C4	10 μ F, 16V	R541062
C5	330pF, 63V	R513315
C6	68pF, 63V	R516905
C7 – C11	10nF, 25V	R501033
C12	10nF, 100V	R521036
C13	10nF, 25V	R501033
C14	10nF, 25V	R501033
C15	10nF, 100V	R521036
C16	10nF, 25V	R501033
C17	10nF, 25V	R501033
C18	10nF, 25V	R501033
C19	47 μ F, 6.3V	R544761
C20	Not fitted	—
C21	47 μ F, 6.3V	R544761
C22	Not fitted	—
C23	10 μ F, 16V	R541062
C24	10 μ F, 16V	R541062
C25	10nF, 25V	R501033
C26	10 μ F, 16V	R541062
C27	10nF, 25V	R501033
C28	10 μ F, 16V	R541062
C29	22pF, 25V	R503303
C30	10nF, 100V	R521036
C31	10nF, 25V	R501033
C32	10 μ F, 16V	R541062
C33	10nF, 25V	R501033
C34	10 μ F, 16V	R541062
C35	33pF, 25V	R503303
C36	10 μ F, 16V	R541062
C37	10nF, 25V	R501033
C38	10nF, 25V	R501033

CIRCUIT REF.	DESCRIPTION	PART NO.
	CAPACITORS (continued)	
C39	100pF, 63V	R511015
C40	10nF, 25V	R501033
C41	560pF, 63V	R515615
C42	10nF, 25V	R501033
C43	82pF, 63V	R518205
C44	Not fitted	—
C45	Not fitted	—
C46	10nF, 25V	R501033
C47	82pF, 63V	R518205
C48	10 μ F, 16V	R541062
C49	10 μ F, 16V	R541062
C50	10nF, 25V	R501033
C51	10nF, 25V	R501033
C52	33pF, 25V	R503303
C53	10nF, 25V	R501033
C54	22 μ F, 35V	R562264
C55	10nF, 25V	R501033
C56	10nF, 25V	R501033
C57	22 μ F, 35V	R562264
C58	10nF, 25V	R501033
C59	10nF, 25V	R501033
C60	100pF, 63V	R511015
C61	22 μ F, 6.3V	R542261
C62	10nF, 25V	R501033
C63	10 μ F, 16V	R541062
C64	220pF, 63V	R512215
C65	Not fitted	—
C66	820pF, 63V	R518215
C67	150pF, 63V	R511515
C68	1000pF, 63V	R511025
C69	100pF, 63V	R511015
C70	10nF, 25V	R501033
C71	10nF, 25V	R501033
C72	10nF, 25V	R501033

CIRCUIT REF.	DESCRIPTION	PART NO.
	CAPACITORS (continued)	
C73	47 μ F, 6.3V	R544761
C74	100nF, 25V	R501043
C75	10nF, 25V	R501033
C76	100nF, 25V	R501043
C77	47 μ F, 6.3V	R544761
C78	10nF, 25V	R501033
C79	22pF, 63V	R512205
C80	10 μ F, 16V	R541062
C81	10 μ F, 16V	R541062
C82	10 μ F, 16V	R541062
C83	10nF, 25V	R501033
C84	Not fitted	—
C85	10nF, 25V	R501033
C86	Not fitted	—
C87	22 μ F, 6.3V	R542261
C88	10nF, 25V	R501033
C89	22pF, 63V	R512205
C90	39pF, 63V	R513905
C91	Not fitted	—
C92	10nF, 25V	R501033
C93	10nF, 25V	R501033
C94	220pF, 63V	R512215
C95	10nF, 25V	R501033
C96	470pF, 63V	R514715
C97	10nF, 25V	R501033
C98	47pF, 63V	R514705
C99	10nF, 25V	R501033
C100	220pF, 63V	R512215
C101	33pF, 63V	R513305
C102	10 μ F, 16V	R541062
C103	Not fitted	—
C104	150pF, 63V	R511515
C105 – C109	10nF, 25V	R501033
C110	220pF, 63V	R512215

CIRCUIT REF.	DESCRIPTION	PART NO.
CAPACITORS (continued)		
C111	Not fitted	—
C112	820pF, 63V	R518215
C113	150pF, 63V	R511515
C114	1000pF, 63V	R511025
C115	100pF, 63V	R511015
C116	100pF, 63V	R511015
C117	100nF, 100V	R521046
C118	22 μ F, 6.3V	R542261
C119	33pF, 63V	R503305
C120	10 μ F, 16V	R541062
C121	220pF, 63V	R512215
C122 – C149	10nF, 25V	R501033
C150	10 μ F, 16V	R541062
C151	10 μ F, 16V	R541062
C152	10nF, 25V	R501033
C153	10nF, 25V	R501033
C200	10nF, 25V	R501033
C201	18pF, 63V	R511805
DELAY LINES		
DL1	VS400	R681400
DL2	VS400	R681400
DIODES		
D1	8.2V 5% Zener 400mW	R399822
D2	6.2V 5% Zener 400mW	R399622
D3	8.2V 5% Zener 400mW	R399822
D4	6.2V 5% Zener 400mW	R399622
D5	6.8V 5% Zener 400mW	R399682
D6	18V 5% Zener 400mW	R399183
D7	4.7V 5% Zener 400mW	R399472
D8	6.8V 5% Zener 400mW	R399682
D9	1N4148	R354148
D10	1N4148	R354148
D11 – D20	1N916	R350916
D21	1N4001	R354001

CIRCUIT REF.	DESCRIPTION	PART NO.
	DIODES (continued)	
D22	1N4001	R354001
D24	8.2V 5% Zener 400mW	R399822
	INTEGRATED CIRCUITS	
IC1	74S175	R230175
IC2	74S175	R230175
IC3	74S374	R230374
IC4	74LS40	R240040
IC5	74LS374	R240374
IC6	74LS374	R249374
IC7	10124	R250124
IC8	10124	R250124
IC9	NE 5007 DAC-08	R285007
IC10	NE 5007 DAC-08	R285007
IC11	74S175	R230175
IC12	74S64	R230064
IC13	74S00	R230000
IC14	74S74	R230074
IC15	74S74	R230074
IC16	10318	R250318
IC17	10176	R250176
IC18	10131	R250131
IC19 – IC25	MC1496N	R281496
IC26	4011B	R261011
IC27	4069B	R261069
IC29	4066B	R261066
IC30	741	R280741
IC31	741	R28-741
	INDUCTORS	
L1	14.23 μ H, Type AF	R600131
L2	26.95 μ H, Type AE	R600131
L3	14.23 μ H, Type AF	R600131
L4	26.95 μ H, Type AE	R600130
L7	68 μ H 5%	R620683
L8	33 μ H 5%	R620339

CIRCUIT REF.	DESCRIPTION	PART NO.
	INDUCTORS (continued)	
L9	47 μ H 5%	R620473
L10	47 μ H 5%	R620473
L11	47 μ H 5%	R620473
	RESISTORS	
R1	1k0 $\pm$ 5%, $\frac{1}{3}$ W	R401105
R2	47K $\pm$ 5%, $\frac{1}{3}$ W	R401476
R3	10k $\pm$ 5%, $\frac{1}{3}$ W	R401106
R4 – R7	47R $\pm$ 5%, $\frac{1}{3}$ W	R401473
R8 – R15	2k2 $\pm$ 5%, $\frac{1}{3}$ W	R401225
R16 – R20	6k8 $\pm$ 5%, $\frac{1}{3}$ W	R401685
R21	15k $\pm$ 5%, $\frac{1}{3}$ W	R401156
R22	6k8 $\pm$ 5%, $\frac{1}{3}$ W	R401685
R23	15k $\pm$ 5%, $\frac{1}{3}$ W	R401156
R26	15k $\pm$ 5%, $\frac{1}{3}$ W	R401156
R27	2k2 $\pm$ 5%, $\frac{1}{3}$ W	R401225
R28	22k $\pm$ 5%, $\frac{1}{3}$ W	R401226
R29	10k $\pm$ 5%, $\frac{1}{3}$ W	R401106
R30	100 $\pm$ 5%, $\frac{1}{3}$ W	R401104
R31	1k0 $\pm$ 5%, $\frac{1}{3}$ W	R401105
R32	1k0 $\pm$ 5%, $\frac{1}{3}$ W	R401105
R33	10R $\pm$ 5%, $\frac{1}{3}$ W	R401103
R34	2k2 $\pm$ 5%, $\frac{1}{3}$ W	R401225
R35	22k $\pm$ 5%, $\frac{1}{3}$ W	R401226
R36	15k $\pm$ 5%, $\frac{1}{3}$ W	R401156
R37	10k $\pm$ 5%, $\frac{1}{3}$ W	R401106
R38	100 $\pm$ 5%, $\frac{1}{3}$ W	R401104
R39	1k0 $\pm$ 5%, $\frac{1}{3}$ W	R401105
R40	1k0 $\pm$ 5%, $\frac{1}{3}$ W	R401105
R41	10R $\pm$ 5%, $\frac{1}{3}$ W	R401103
R42	15k $\pm$ 5%, $\frac{1}{3}$ W	R401156
R43	15k $\pm$ 5%, $\frac{1}{3}$ W	R401156
R44	27k $\pm$ 5%, $\frac{1}{3}$ W	R401276
R45	27k $\pm$ 5%, $\frac{1}{3}$ W	R401276
R46	680 $\pm$ 5%, $\frac{1}{3}$ W	R401684

CIRCUIT REF.	DESCRIPTION	PART NO.
	RESISTORS (continued)	
R47	33R $\pm 5\%$, $\frac{1}{3}$ W	R401333
R48	33R $\pm 5\%$, $\frac{1}{3}$ W	R401333
R50	33R $\pm 5\%$, $\frac{1}{3}$ W	R401333
R51	1k0 $\pm 5\%$, $\frac{1}{3}$ W	R401105
R52	1k0 $\pm 5\%$, $\frac{1}{3}$ W	R401105
R53	100 $\pm 5\%$, $\frac{1}{3}$ W	R401104
R54	33R $\pm 5\%$, $\frac{1}{3}$ W	R401333
R55	680 $\pm 5\%$, $\frac{1}{3}$ W	R401684
R56	33R $\pm 5\%$, $\frac{1}{3}$ W	R401333
R57	1k0 $\pm 5\%$, $\frac{1}{3}$ W	R401105
R58	100 $\pm 5\%$, $\frac{1}{3}$ W	R401104
R59	1k0 $\pm 5\%$, $\frac{1}{3}$ W	R401105
R60	33R $\pm 5\%$, $\frac{1}{3}$ W	R401333
R61	2k2 $\pm 5\%$, $\frac{1}{3}$ W	R401225
R62	22k $\pm 5\%$, $\frac{1}{3}$ W	R401226
R63	500 $\pm 5\%$, $\frac{1}{3}$ W	R401564
R64	22k $\pm 5\%$, $\frac{1}{3}$ W	R401226
R65	2k2 $\pm 5\%$, $\frac{1}{3}$ W	R401225
R66	8k2 $\pm 5\%$, $\frac{1}{3}$ W	R401825
R67	10k $\pm 5\%$, $\frac{1}{3}$ W	R401106
R68	56k $\pm 5\%$, $\frac{1}{3}$ W	R401566
R69	1k0 $\pm 5\%$, $\frac{1}{3}$ W	R401105
R70	270 $\pm 5\%$, $\frac{1}{3}$ W	R401274
R71	15k $\pm 5\%$, $\frac{1}{3}$ W	R401156
R72	1k2 $\pm 5\%$, $\frac{1}{3}$ W	R401125
R73	3k3 $\pm 5\%$, $\frac{1}{3}$ W	R401335
R74	12k $\pm 5\%$, $\frac{1}{3}$ W	R401126
R75	100 $\pm 5\%$, $\frac{1}{3}$ W	R401104
R76	27k $\pm 5\%$, $\frac{1}{3}$ W	R401276
R77	560 $\pm 5\%$, $\frac{1}{3}$ W	R401564
R78	10k $\pm 5\%$, $\frac{1}{3}$ W	R401106
R79	150 $\pm 5\%$, $\frac{1}{3}$ W	R401154
R80	820 $\pm 5\%$, $\frac{1}{3}$ W	R401824
R81	2k2 $\pm 5\%$, $\frac{1}{3}$ W	R401225

CIRCUIT REF.	DESCRIPTION	PART NO.
	RESISTORS (continued)	
R82	2k2 $\pm 5\%$, $\frac{1}{3}$ W	R401225
R83	680 $\pm 5\%$, $\frac{1}{3}$ W	R401684
R86	4k7 $\pm 5\%$, $\frac{1}{3}$ W	R401475
R87	10k $\pm 5\%$, $\frac{1}{3}$ W	R401106
R88	56k $\pm 5\%$, $\frac{1}{3}$ W	R401566
R89	1k0 $\pm 5\%$, $\frac{1}{3}$ W	R401105
R90	270 $\pm 5\%$, $\frac{1}{3}$ W	R401274
R91	15k $\pm 5\%$, $\frac{1}{3}$ W	R401156
R92	27k $\pm 5\%$, $\frac{1}{3}$ W	R401276
R93	1k2 $\pm 5\%$, $\frac{1}{3}$ W	R401125
R94	3k3 $\pm 5\%$, $\frac{1}{3}$ W	R401335
R95	12k $\pm 5\%$, $\frac{1}{3}$ W	R401126
R96	100 $\pm 5\%$, $\frac{1}{3}$ W	R401104
R97	10k $\pm 5\%$, $\frac{1}{3}$ W	R401106
R98	560 $\pm 5\%$, $\frac{1}{3}$ W	R401564
R99	150 $\pm 5\%$, $\frac{1}{3}$ W	R401154
R100	820 $\pm 5\%$, $\frac{1}{3}$ W	R401824
R101	2k2 $\pm 5\%$, $\frac{1}{3}$ W	R401225
R102	2k2 $\pm 5\%$, $\frac{1}{3}$ W	R401225
R103	2k2 $\pm 5\%$, $\frac{1}{3}$ W	R401225
R104	1k0 $\pm 5\%$, $\frac{1}{3}$ W	R401105
R105	330 $\pm 5\%$, $\frac{1}{3}$ W	R401334
R106	Not fitted	—
R107	470 $\pm 5\%$, $\frac{1}{3}$ W	R401474
R108	10k $\pm 5\%$, $\frac{1}{3}$ W	R401106
R109	4k7 $\pm 5\%$, $\frac{1}{3}$ W	R401475
R110	2k2 $\pm 5\%$, $\frac{1}{3}$ W	R401225
R111	Not fitted	—
R112	100 $\pm 5\%$, $\frac{1}{3}$ W	R401104
R113	100 $\pm 5\%$, $\frac{1}{3}$ W	R401104
R114	100 $\pm 5\%$, $\frac{1}{3}$ W	R401104
R115	470 $\pm 5\%$, $\frac{1}{3}$ W	R401474
R116	270 $\pm 5\%$, $\frac{1}{3}$ W	R401274
R117	2k2 $\pm 5\%$, $\frac{1}{3}$ W	R401225

CIRCUIT REF.	DESCRIPTION	PART NO.
	RESISTORS (continued)	
R118	10k $\pm 5\%$, $\frac{1}{3}$ W	R401106
R119	1k5 $\pm 5\%$, $\frac{1}{3}$ W	R401155
R120	22k $\pm 5\%$, $\frac{1}{3}$ W	R401226
R121	22k $\pm 5\%$, $\frac{1}{3}$ W	R401226
R122	100 $\pm 5\%$, $\frac{1}{3}$ W	R401104
R123	100 $\pm 5\%$, $\frac{1}{3}$ W	R401104
R124	100 $\pm 5\%$, $\frac{1}{3}$ W	R401104
R125	1k0 $\pm 5\%$, $\frac{1}{3}$ W	R401105
R126	4k7 $\pm 5\%$, $\frac{1}{3}$ W	R401475
R127 – R132	1k0 $\pm 5\%$, $\frac{1}{3}$ W	R401105
R133	27k $\pm 5\%$, $\frac{1}{3}$ W	R401276
R134	4k7 $\pm 5\%$, $\frac{1}{3}$ W	R401475
R135	2k2 $\pm 5\%$, $\frac{1}{3}$ W	R401225
R136	56k $\pm 5\%$, $\frac{1}{3}$ W	R401566
T137	1k0 $\pm 5\%$, $\frac{1}{3}$ W	R401105
R138	10k $\pm 5\%$, $\frac{1}{3}$ W	R401106
R139	220 $\pm 5\%$, $\frac{1}{3}$ W	R401224
R140	15k $\pm 5\%$, $\frac{1}{3}$ W	R401156
R141	220 $\pm 5\%$, $\frac{1}{3}$ W	R401224
R142	27k $\pm 5\%$, $\frac{1}{3}$ W	R401276
R143	150 $\pm 5\%$, $\frac{1}{3}$ W	R401154
R144	2k2 $\pm 5\%$, $\frac{1}{3}$ W	R401225
R145	3k3 $\pm 5\%$, $\frac{1}{3}$ W	R401335
R146	12k $\pm 5\%$, $\frac{1}{3}$ W	R401126
R147	68R $\pm 5\%$, $\frac{1}{3}$ W	R401683
R148	56R $\pm 5\%$, $\frac{1}{3}$ W	R401563
R149	100 $\pm 5\%$, $\frac{1}{3}$ W	R401104
R150	560 $\pm 5\%$, $\frac{1}{3}$ W	R401564
R151	120 $\pm 5\%$, $\frac{1}{3}$ W	R401124
R152	75R $\pm 1\%$, 0.4W	R432753
R153	100 $\pm 5\%$, $\frac{1}{3}$ W	R401104
R154	100 $\pm 5\%$, $\frac{1}{3}$ W	R401104
R155	560 $\pm 5\%$, $\frac{1}{3}$ W	R401564
R156	220k $\pm 5\%$, $\frac{1}{3}$ W	R401227

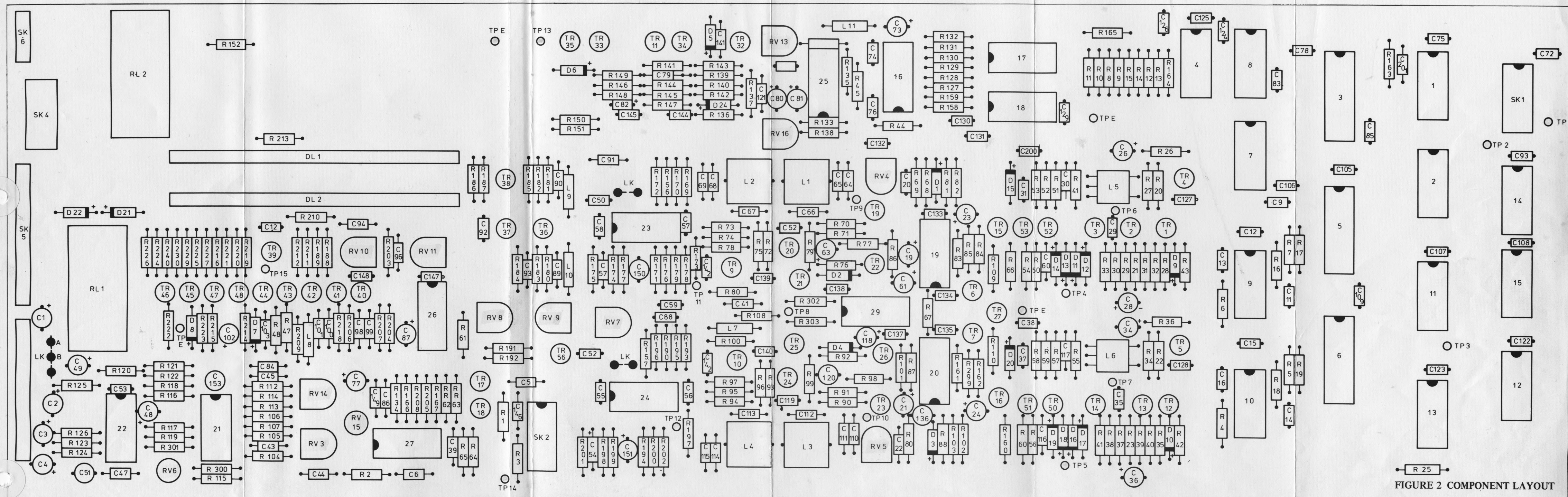
CIRCUIT REF.	DESCRIPTION	PART NO.
	RESISTORS (continued)	
R157	220k $\pm 5\%$, $\frac{1}{3}$ W	R401227
R158	1k0 $\pm 5\%$, $\frac{1}{3}$ W	R401105
R159	1k0 $\pm 5\%$, $\frac{1}{3}$ W	R401105
R160	8k2 $\pm 5\%$, $\frac{1}{3}$ W	R401825
R161	680 $\pm 5\%$, $\frac{1}{3}$ W	R401684
R162	Not fitted	—
R163	2k2 $\pm 5\%$, $\frac{1}{3}$ W	R401225
R164	3k9 $\pm 5\%$, $\frac{1}{3}$ W	R401395
R165	1k2 $\pm 5\%$, $\frac{1}{3}$ W	R401125
R166	470 $\pm 5\%$, $\frac{1}{3}$ W	R401474
R167	22k $\pm 5\%$, $\frac{1}{3}$ W	R401226
R169	22k $\pm 5\%$, $\frac{1}{3}$ W	R401226
R170	10k $\pm 5\%$, $\frac{1}{3}$ W	R401106
R171	22k $\pm 5\%$, $\frac{1}{3}$ W	R401226
R172	1k0 $\pm 5\%$, $\frac{1}{3}$ W	R401105
R173	470 $\pm 5\%$, $\frac{1}{3}$ W	R401474
R174	680 $\pm 5\%$, $\frac{1}{3}$ W	R401684
R175	100 $\pm 5\%$, $\frac{1}{3}$ W	R401104
R176	4k7 $\pm 5\%$, $\frac{1}{3}$ W	R401475
R177	390 $\pm 5\%$, $\frac{1}{3}$ W	R401394
R178	47R $\pm 5\%$, $\frac{1}{3}$ W	R401473
R179	1k0 $\pm 5\%$, $\frac{1}{3}$ W	R401105
R180	100 $\pm 5\%$, $\frac{1}{3}$ W	R401104
R181	100 $\pm 5\%$, $\frac{1}{3}$ W	R401104
R182	1k5 $\pm 5\%$, $\frac{1}{3}$ W	R401155
R183	1k5 $\pm 5\%$, $\frac{1}{3}$ W	R401155
R184	2k2 $\pm 5\%$, $\frac{1}{3}$ W	R401225
R185	100 $\pm 5\%$, $\frac{1}{3}$ W	R401104
R186	1k2 $\pm 5\%$, $\frac{1}{3}$ W	R401125
R187	1k0 $\pm 5\%$, $\frac{1}{3}$ W	R401105
R188	2k2 $\pm 5\%$, $\frac{1}{3}$ W	R401225
R189	2k7 $\pm 5\%$, $\frac{1}{3}$ W	R401275
R190	1k0 $\pm 5\%$, $\frac{1}{3}$ W	R401105
R191	4k7 $\pm 5\%$, $\frac{1}{3}$ W	R401475

CIRCUIT REF.	DESCRIPTION	PART NO.
	RESISTORS (continued)	
R192	10k $\pm$ 5%, $\frac{1}{3}$ W	R401106
R193	22k $\pm$ 5%, $\frac{1}{3}$ W	R401226
R194	22k $\pm$ 5%, $\frac{1}{3}$ W	R401226
R195	10k $\pm$ 5%, $\frac{1}{3}$ W	R401106
R196	1k0 $\pm$ 5%, $\frac{1}{3}$ W	R401105
R197	470 $\pm$ 5%, $\frac{1}{3}$ W	R401474
R198	680 $\pm$ 5%, $\frac{1}{3}$ W	R401684
R199	100 $\pm$ 5%, $\frac{1}{3}$ W	R401104
R200	4k7 $\pm$ 5%, $\frac{1}{3}$ W	R401475
R201	100 $\pm$ 5%, $\frac{1}{3}$ W	R401104
R202	10k $\pm$ 5%, $\frac{1}{3}$ W	R401106
R203	4k7 $\pm$ 5%, $\frac{1}{3}$ W	R401475
R204	15k $\pm$ 5%, $\frac{1}{3}$ W	R401156
R205	1k0 $\pm$ 5%, $\frac{1}{3}$ W	R401105
R206	560 $\pm$ 5%, $\frac{1}{3}$ W	R401564
R207	15k $\pm$ 5%, $\frac{1}{3}$ W	R401156
R208	22k $\pm$ 5%, $\frac{1}{3}$ W	R401226
R209	2k2 $\pm$ 5%, $\frac{1}{3}$ W	R401225
R210	390 $\pm$ 5%, $\frac{1}{3}$ W	R401394
R211	2k7 $\pm$ 5%, $\frac{1}{3}$ W	R401275
R212	220 $\pm$ 5%, $\frac{1}{3}$ W	R401224
R213	75R $\pm$ 1%, 0.4W	R432753
R214	4k9 $\pm$ 5%, $\frac{1}{3}$ W	R401475
R215	560 $\pm$ 5%, $\frac{1}{3}$ W	R401564
R216	8k2 $\pm$ 5%, $\frac{1}{3}$ W	R401825
R218	1k0 $\pm$ 5%, $\frac{1}{3}$ W	R401105
R219	2k2 $\pm$ 5%, $\frac{1}{3}$ W	R401225
R220	120 $\pm$ 5%, $\frac{1}{3}$ W	R401124
R221	120 $\pm$ 5%, $\frac{1}{3}$ W	R401124
R222	470 $\pm$ 5%, $\frac{1}{3}$ W	R401474
R223	470 $\pm$ 5%, $\frac{1}{3}$ W	R401474
R224	150 $\pm$ 1%, 0.4W	R432154
R225	150 $\pm$ 1%, 0.4W	R432154
R226	150 $\pm$ 1%, 0.4W	R432154

CIRCUIT REF.	DESCRIPTION	PART NO.
	RESISTORS (continued)	
R227	150 $\pm$ 1%, 0.4W	R432154
R229	560 $\pm$ 5%, $\frac{1}{3}$ W	R401564
R230	2k2 $\pm$ 5%, $\frac{1}{3}$ W	R401225
R240	6k8 $\pm$ 5%, $\frac{1}{3}$ W	R401685
R299	Not fitted	—
R300	10k $\pm$ 5%, $\frac{1}{3}$ W	R401106
R301	100k $\pm$ 5%, $\frac{1}{3}$ W	R401107
R302	100 $\pm$ 5%, $\frac{1}{3}$ W	R401104
R303	100 $\pm$ 5%, $\frac{1}{3}$ W	R401104
R304	2k2 $\pm$ 5%, $\frac{1}{3}$ W	R401225
RV3	1k0, variable	R492105
RV4	10k, variable	R492106
RV5	10k, variable	R492106
RV6	50k, variable	R495506
RV7	47k, variable	R492476
RV8	47k, variable	R492476
RV9	1k0, variable	R492105
RV10	4k7, variable	R492475
RV11	4k7, variable	R492475
RV13	4k7, variable	R492475
RV14	4k7, variable	R492475
RV15	5k0, variable	R495505
RV16	22k, variable	R492226
	RELAYS	
RL1	NF2, 6V coil	R790062
RL2	NF2, 6V coil	R790062
	CONNECTORS	
SK1	Socket, 16-pin DIL	R808016
SK2	Socket, 16-pin DIL	R808016
SK3	2-part connector, 15 pins	R810015
SK4	Socket, 16-pin DIL	R808016
SK5	2-part connector, 15 pins	R810015
SK6	2-part connector, 5 pins	R810005

CIRCUIT REF.	DESCRIPTION	PART NO.
	TRANSFORMERS	
T1	10/5 + 5	R650132
T2	10/5 + 5	R650132
T3	10/5 + 5	R650132
	TRANSISTORS	
TR1	ZTX107L	R348107
TR2	ZTX212AL	R348212
TR3	ZTX212AL	R348212
TR4	ZTX212AL	R348212
TR5	ZTX212AL	R348212
TR9	ZTX212AL	R348212
TR10	ZTX212AL	R348212
TR11	ZTX212AL	R348212
TR12	ZTX107L	R348107
TR13	ZTX212AL	R348212
TR14	ZTX212AL	R348212
TR15	E210	R325210
TR16	E210	R325210
TR17	ZRX212AL	R348212
TR18	ZTX212AL	R348212
TR19	ZTX107L	R348107
TR20	ZTX212AL	R348212
TR21	ZTX107L	R348107
TR22	ZTX107L	R348107
TR23	ZTX107L	R348107
TR24	ZTX212AL	R348212
TR25	ZTX107L	R348107
TR26	ZTX107L	R348107
TR27	ZTX212AL	R348212
TR32	ZTX107L	R348107
TR33	2N2219	R302219
TR34	ZTX212AL	R348212
TR35	2N2219	R302219
TR36	ZTX107L	R348107
TR37	ZTX212AL	R348212

CIRCUIT REF.	DESCRIPTION	PART NO.
	TRANSISTORS (continued)	
TR38	ZTX107L	R348107
TR39	ZTX212AL	R348212
TR40	ZTX212AL	R348212
TR41	ZTX212AL	R348212
TR42	ZTX107L	R348107
TR43	ZTX107L	R348107
TR44	ZTX107L	R348107
TR45	ZTX107L	R348107
TR46	2N2219	R302219
TR47	2N2905	R302905
TR48	ZTX212AL	R348212
TR50	2N2369A	R312369
TR51	2N2369A	R312369
TR52	2N2369A	R312369
TR53	2N2369A	R312369
TR56	ZTX212AL	R348212



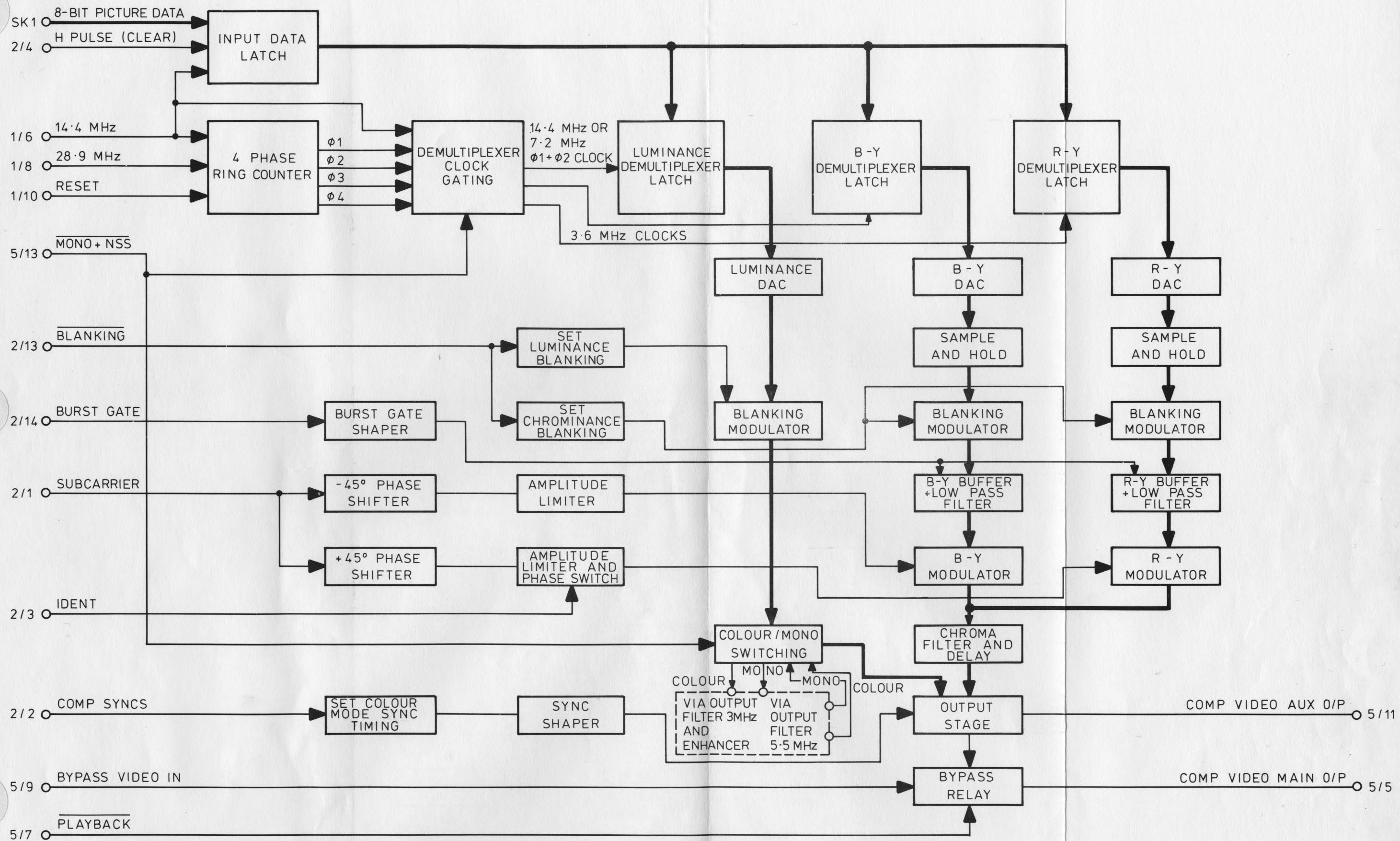


FIGURE 1 BLOCK DIAGRAM

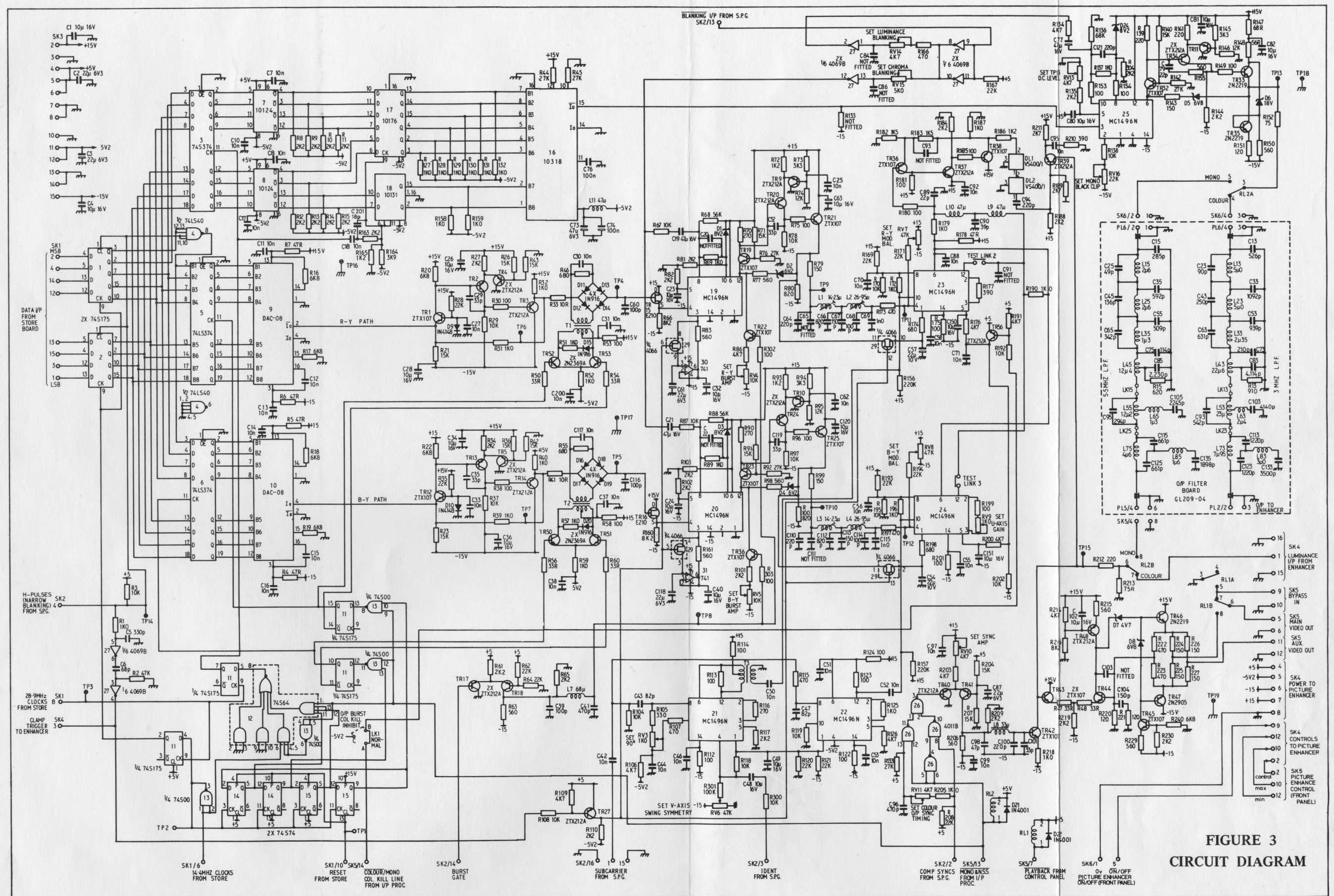


FIGURE 3
CIRCUIT DIAGRAM

ENHANCER

ENHANCER
IVC PCB GL210

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TEST POINTS	2
COMPONENT SCHEDULE	3

FIGURE 1	BLOCK DIAGRAM
FIGURE 2	COMPONENT LAYOUT
FIGURE 3	CIRCUIT DIAGRAM

ENHANCER

IVC PCB GL210

INTRODUCTION

The Enhancer card provides an adjustable high frequency response in the luminance channel (colour mode only) to produce enhancement of detail in the "off tape" signal.

This is accomplished by splitting the 3MHz band limited luminance signal into two paths. One path is through a 1.5MHz gaussian low pass filter, while the other is through a delay line which provides a delay equal to the low pass filter. The 1.5MHz filtered signal is then subtracted from the delayed signal to produce a "detail" signal with frequencies in the range 1.5MHz to 3MHz.

This high frequency detail signal is then fed through a threshold circuit which only allows signals greater than a preset level to pass. This process, known as "noise coring", ensures that as the detail signal amplitude is increased, high frequency noise components are not amplified in flat areas of the picture.

The "cored" signal is then passed through an amplifier whose gain is controlled from the front panel. The output from this amplifier is combined with the 1.5MHz low pass filtered signal to form an "enhanced" luminance signal. This is clamped to establish a dc level, and passed through a peak white and black level clipper. The output is provided through a 75ohm output stage.

CIRCUIT DESCRIPTION

The 3MHz band limited luminance signal from the Output Filter card enters the Enhancer card at SK2/2 and is amplified by buffer amplifier TR1, TR2, TR3. The signal is then fed both to a gaussian low pass filter (L6, L7, C3, C4, C5) and a delay line with a 5MHz bandwidth (L1-L5, C6-C11). The filtered signal and the delayed signal are then fed to subtractor IC1, the delayed signal via gain adjustment potentiometer RV1. This is adjusted

for a null of low frequency signals at the output of the subtractor, IC1 pin 12. This output is the "detail" signal and passes, via emitter follower TR4, to the noise corer circuit comprising IC2, TR5, TR6, D1, D2 and TR17.

The detail signal is monitored at TP2, and C13, L8 ensure that the mean level is 0V. Diodes D1 and D2 are forward biased by the negative or positive edges of the detail signal when they exceed a certain threshold voltage. The positive side of the threshold voltage is controlled by current source TR6, and the negative side by TR5. These current sources are ganged together via a "mirror" arrangement (TR7, R26), and the threshold voltage may be adjusted by potentiometer RV2 which changes the current through R24 from TR6. The positive and negative halves of the detail signal are then summed at the collectors of TR8 and TR9, and coupled via C17 to the X inputs of analogue multiplier IC3. The dc level on these inputs is determined by R34 and R35. The Y inputs, on IC3 pins 4 and 8, are derived from the PICTURE ENHANCE control on the front panel (via SK1/10), and from potentiometer RV3. This is used to adjust the multiplier gain for a flat overall frequency response of the enhancer when the front panel control is fully counter-clockwise but not switched off. The detailed signal output from IC3 pin 2 is in current form.

When enhancement control is selected on the front panel, relay RL1 is energised via SK1/9 and switches the 1.5MHz low pass filtered signal through to the base of TR10. When enhancement control is not selected and RL1 is de-energised, the delayed 3MHz luminance signal is switched through. TR10, TR11 and TR12 form a feedback amplifier with the gain adjustable by RV4. The signal from IC3/2 is summed at the emitter of TR10 with the signal selected by RL1. The combined signal appears at the emitter of TR12 and is coupled via clamp capacitor C25 to diode bridge D3-D6.

The CLAMP signal enters the Enhancer card at SK1/3 and triggers monostable IC5 whose output at IC5/10 is normally high and goes low during the clamp pulse period. When it is high, TR13 and TR14 are switched on and no current flows into C23 and C24. Diode bridge D3-D6 is reverse biased and the clamp circuit is inhibited. When IC5/10 goes low, TR13 and TR14 are turned off and the current through R54 flows through C24, the diode bridge, C23 and R55. The bridge is forward biased and the combined signal (monitored at TP4) is clamped to OV.

The luminance signal, with its blanking level clamped to OV, is now fed to pin 1 of transistor array IC4. The transistor with emitter at pin 2 is an emitter follower with emitter resistor R58. The transistor with emitter at pin 7 clips negative-going signals at a level set by potentiometer RV5. The signal passes through R59 to the emitter of a PNP transistor (IC4/10) which clips the positive-going signals at a level determined by potentiometer RV6. The signal then passes via R60 to the base of output transistor TR15. TR16 forms an active current source for this emitter follower.

The output signal, monitored at TP6, is coupled via a 75 ohm output resistor R64 to SK1/1.

ADJUSTMENTS

VR1 – Adjusts the balance of subtractor IC1. With a probe on IC1 pin 12, adjust VR1 for null of low frequency components of the luminance signal.

VR2 – Adjusts the noise coring level of the detail signal.

VR3 – Adjusts the enhancement control range. Set RV3 so that 2T pulse to bar ratio is the same with the front panel PICTURE ENHANCE control switched off and just switched on.

VR4 – Sets the overall luminance gain of the enhancer. It is adjusted so the luminance level at the output of the TBC-2002 is the same when switching between monochrome and colour on the front panel.

VR5 – Adjusts the negative clipping level of the luminance signal. It is set to clip at -75mV below black level at the output.

VR6 – Adjusts the positive clipping level of the luminance signal. It is set to clip at +75mV above peak white at the output.

VR7 – Sets the dc level of the enhanced luminance signal. With a probe on the emitter of TR12 and R51, adjust RV7 for black level at -2V when the PICTURE ENHANCE control on the front panel is switched on.

VR8 – Sets the clamp pulse width. This is nominally 6ms.

VR9 – Sets luminance gain with ENHANCE control off
CONNECTIONS

SK1	Control Signals
1	Video output
2	PICTURE ENHANCE, -15V
3	CLAMP I/P
4	+5V
6	-15V
7	+15V
8	OV
9	PICTURE ENHANCE $\overline{\text{ON}}$ /OFF
10	PICTURE ENHANCE control
12	PICTURE ENHANCE, ground
15	Video output, ground
16	Video output, ground

SK2	Video Signal
1	Video input, ground
2	Video input,
3	Video input, ground

TEST POINTS

TP1	Buffer amplifier output
TP2	Detail signal
TP3	Noise cored signal
TP4	Enhanced luminance signal
TP5	Luminance signal at output of relay RL1
TP6	Output video
TP7	Clamp monostable output

CIRCUIT REF.	DESCRIPTION	PART NO.
	CAPACITORS	
C1	Not fitted	—
C2	10 μ F, 16V	R541062
C3	1200pF $\pm$ 5%, 63V	R511225
C4	470pF $\pm$ 5%, 63V	R514715
C5	100pF $\pm$ 5%, 63V	R511015
C6	120pF $\pm$ 5%, 63V	R511215
C7	270pF $\pm$ 5%, 63V	R512715
C8	270pF $\pm$ 5%, 63V	R512715
C9	270pF $\pm$ 5%, 63V	R512715
C10	270pF $\pm$ 5%, 63V	R512715
C11	120pF $\pm$ 5%, 63V	R511215
C12	10nF, 25V	R501033
C13	100nF, 100V	R521046
C14	10nF, 25V	R501033
C15	10nF, 25V	R501033
C16	10nF, 25V	R501033
C17	100nF, 100V	R521046
C18	10 μ F, 16V	R541062
C19	10nF, 25V	R501033
C20	10nF, 25V	R501033
C21	10pF, 63V	R511034
C22	Not fitted	—
C23	47nF, 100V	R524736
C24	47nF, 100V	R524736
C25	220nF, 63V	R522245
C26	Not fitted	—
C27	10nF, 25V	R501033
C28	10 μ F, 16V	R541062
C29	10 μ F, 16V	R541062
C30	10 μ F, 16V	R541062
C31	22 μ F, 6.3V	R542261
C32	Not fitted	—
C33	10 μ F, 16V	R541062
C34	10 μ F, 16V	R541062

CIRCUIT REF.	DESCRIPTION	PART NO.
	CAPACITORS (continued)	
C35	10nF, 25V	R501033
C36	120pF $\pm 5\%$, 63V	R511215
C37	120pF $\pm 5\%$, 63V	R511215
C38	10nF, 25V	R501033
C39	10 μ F, 6.3V	R541061
C40	56pF, 63V	R515605
C41	10nF, 25V	R501033
C42	10nF, 25V	R501033
C43	10nF, 25V	R501033
C44	22pF, 63V	R512205
	DIODES	
D1	1N4148	R354148
D2	1N4148	R354148
D3	1N916	R350916
D4	1N916	R350916
D5	1N916	R350916
D6	1N916	R350916
D7	ZF18	R398018
D8	1N4001 or 1N4003	R354001 R354003
D9	ZF4.7	R398047
D10	OA47	R385047
D11	OA47	R385047
	INTEGRATED CIRCUITS	
IC1	1496	R281496
IC2	1458	R281458
IC3	1495	R281495
IC4	CA3096	R283096
IC5	4011	R261011
	INDUCTORS	
L1	10 μ H	R620103
L2	10 μ H	R620103
L3	10 μ H	R620103
L4	10 μ H	R620103

CIRCUIT REF.	DESCRIPTION	PART NO.
	INDUCTORS (continued)	
L5	10 μ H	R620103
L6	22 μ H	R620223
L7	10 μ H	R620103
L8	330 μ H	R620334
L9	10 μ H	R620103
	RESISTORS	
R1	75R $\pm$ 1%, 0.4W	R432753
R2	2k2 $\pm$ 5%, $\frac{1}{3}$ W	R401225
R3	150 $\pm$ 5%, $\frac{1}{3}$ W	R401154
R4	3k3 $\pm$ 5%, $\frac{1}{3}$ W	R401335
R5	1k0 $\pm$ 5%, $\frac{1}{3}$ W	R401105
R6	10k $\pm$ 5%, $\frac{1}{3}$ W	R401106
R7	3k3 $\pm$ 5%, $\frac{1}{3}$ W	R401335
R8	680 $\pm$ 5%, $\frac{1}{3}$ W	R401684
R9	180 $\pm$ 5%, $\frac{1}{3}$ W	R401184
R10	180 $\pm$ 5%, $\frac{1}{3}$ W	R401184
R11	33R $\pm$ 5%, $\frac{1}{3}$ W	R401333
R12	150 $\pm$ 5%, $\frac{1}{3}$ W	R401154
R13	15k $\pm$ 5%, $\frac{1}{3}$ W	R401156
R14	2k2 $\pm$ 5%, $\frac{1}{3}$ W	R401225
R15	15k $\pm$ 5%, $\frac{1}{3}$ W	R401156
R16	100 $\pm$ 5%, $\frac{1}{3}$ W	R401104
R17	2k2 $\pm$ 5%, $\frac{1}{3}$ W	R401225
R18	100 $\pm$ 5%, $\frac{1}{3}$ W	R401104
R19	220 $\pm$ 5%, $\frac{1}{3}$ W	R401224
R20	8k2 $\pm$ 5%, $\frac{1}{3}$ W	R401825
R21	1k0 $\pm$ 5%, $\frac{1}{3}$ W	R401105
R22	10k $\pm$ 5%, $\frac{1}{3}$ W	R401106
R23	1k0 $\pm$ 5%, $\frac{1}{3}$ W	R401105
R24	1k0 $\pm$ 5%, $\frac{1}{3}$ W	R401105
R25	10k $\pm$ 5%, $\frac{1}{3}$ W	R401106
R26	10k $\pm$ 5%, $\frac{1}{3}$ W	R401106
R27	10k $\pm$ 5%, $\frac{1}{3}$ W	R401106
R28	10k $\pm$ 5%, $\frac{1}{3}$ W	R401106

CIRCUIT REF.	DESCRIPTION	PART NO.
	RESISTORS (continued)	
R29	1k0 $\pm 5\%$, $\frac{1}{3}W$	R401105
R30	2k2 $\pm 5\%$, $\frac{1}{3}W$	R401225
R31	2k2 $\pm 5\%$, $\frac{1}{3}W$	R401225
R32	2k2 $\pm 5\%$, $\frac{1}{3}W$	R401225
R33	4k7 $\pm 5\%$, $\frac{1}{3}W$	R401475
R34	10k $\pm 5\%$, $\frac{1}{3}W$	R401106
R35	5k6 $\pm 5\%$, $\frac{1}{3}W$	R401565
R36	4k7 $\pm 5\%$, $\frac{1}{3}W$	R401475
R37	1k0 $\pm 5\%$, $\frac{1}{3}W$	R401105
R38	1k0 $\pm 5\%$, $\frac{1}{3}W$	R401105
R39	390 $\pm 5\%$, $\frac{1}{3}W$	R401394
R40	10k $\pm 5\%$, $\frac{1}{3}W$	R401106
R41	4k7 $\pm 5\%$, $\frac{1}{3}W$	R401475
R42	220k $\pm 5\%$, $\frac{1}{3}W$	R401224
R43	100k $\pm 5\%$, $\frac{1}{3}W$	R401107
R44	390k $\pm 5\%$, $\frac{1}{3}W$	R401397
R45	180k $\pm 5\%$, $\frac{1}{3}W$	R401187
R46	100 $\pm 5\%$, $\frac{1}{3}W$	R401104
R47	100 $\pm 5\%$, $\frac{1}{3}W$	R401104
R48	6k8 $\pm 5\%$, $\frac{1}{3}W$	R401685
R49	4k7 $\pm 5\%$, $\frac{1}{3}W$	R401475
R50	470 $\pm 5\%$, $\frac{1}{3}W$	R401474
R51	3k3 $\pm 5\%$, $\frac{1}{3}W$	R401335
R52	1k0 $\pm 5\%$, $\frac{1}{3}W$	R401105
R53	100 $\pm 5\%$, $\frac{1}{3}W$	R401104
R54	150k $\pm 5\%$, $\frac{1}{3}W$	R401157
R55	5k6 $\pm 5\%$, $\frac{1}{3}W$	R401565
R56	10k $\pm 5\%$, $\frac{1}{3}W$	R401106
R57	5k6 $\Omega \pm 5\%$, $\frac{1}{3}W$	R401565
R58	15k $\pm 5\%$, $\frac{1}{3}W$	R401156
R59	470 $\pm 5\%$, $\frac{1}{3}W$	R401474
R60	100 $\pm 5\%$, $\frac{1}{3}W$	R401104
R61	560 $\pm 5\%$, $\frac{1}{3}W$	R401564
R62	75R $\pm 1\%$, 0.4W	R432753

CIRCUIT REF.	DESCRIPTION	PART NO.
	RESISTORS (continued)	
R63	56R $\pm 5\%$, $\frac{1}{3}$ W	R401563
R64	75R $\pm 1\%$, 0.4W	R432753
R65	47R $\pm 5\%$, $\frac{1}{3}$ W	R401473
R66	68R $\pm 5\%$, $\frac{1}{3}$ W	R401683
R67	1k0 $\pm 5\%$, $\frac{1}{3}$ W	R401105
R68	22k $\pm 5\%$, $\frac{1}{3}$ W	R401226
R69	10k $\pm 5\%$, $\frac{1}{3}$ W	R401106
R70	33k $\pm 5\%$, $\frac{1}{3}$ W	R401336
R71	33k $\pm 5\%$, $\frac{1}{3}$ W	R401336
R72	1k5 $\pm 5\%$, $\frac{1}{3}$ W	R401155
R73	180 $\pm 5\%$, $\frac{1}{3}$ W	R401184
R74	180 $\pm 5\%$, $\frac{1}{3}$ W	R401184
R75	47R $\pm 5\%$, $\frac{1}{3}$ W	R401473
R76	4k7 $\pm 5\%$, $\frac{1}{3}$ W	R401475
R77	560 $\pm 5\%$, $\frac{1}{3}$ W	R401564
R78	330 $\pm 5\%$, $\frac{1}{3}$ W	R401334
RV1	47R, variable	R496473
RV2	10k, variable	R494106
RV3	100k, variable	R492107
RV4	4k7, variable	R492475
RV5	4k7, variable	R492475
RV6	4k7, variable	R492475
RV7	470, variable	R492474
RV8	47k, variable	R492476
	RELAY	
RL1	6V coil	R790051
	CONNECTORS	
SK1	Socket, 16-pin, DIL	R808016
SK2	2-part connector, 3-way	R810103
	TRANSISTORS	
TR1	ZTX107L	R348107
TR2	ZTX212AL	R348212
TR3	ZTX107L	R348107
TR4	ZTX107L	R348107

CIRCUIT REF.	DESCRIPTION	PART NO.
	TRANSISTORS (continued)	
TR5	ZTX212AL	R348212
TR6	ZTX107L	R348107
TR7	ZTX107L	R348107
TR8	ZTX212AL	R348212
TR9	ZTX212AL	R348212
TR10	ZTX107L	R348107
TR11	ZTX212AL	R348212
TR12	ZTX107L	R348107
TR13	ZTX107L	R348107
TR14	ZTX212AL	R348212
TR15	2N2905	R302905
TR16	2N2905	R302905
TR17	ZTX212AL	R348212
TR18	ZTX107L	R348107

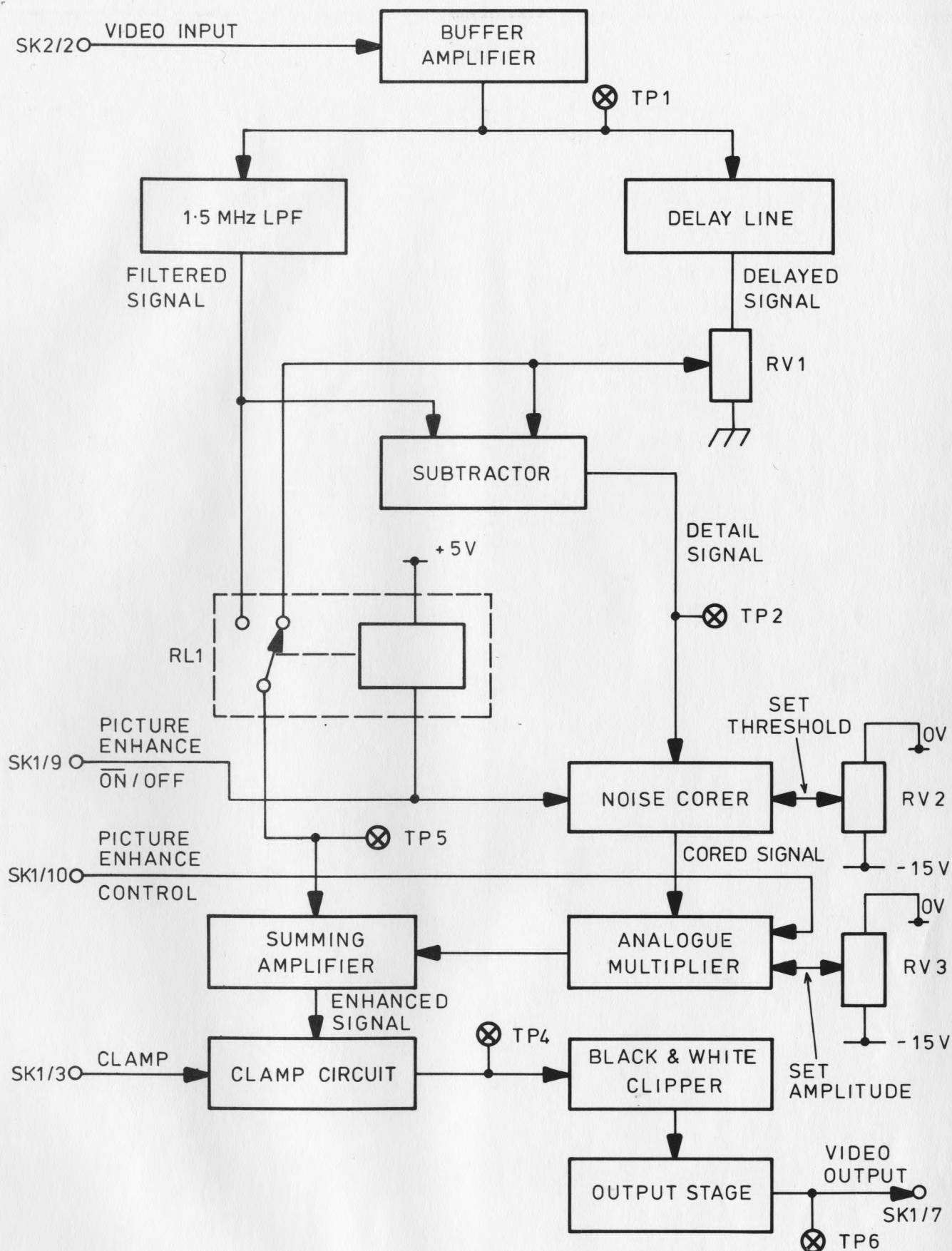


FIGURE 1 BLOCK DIAGRAM

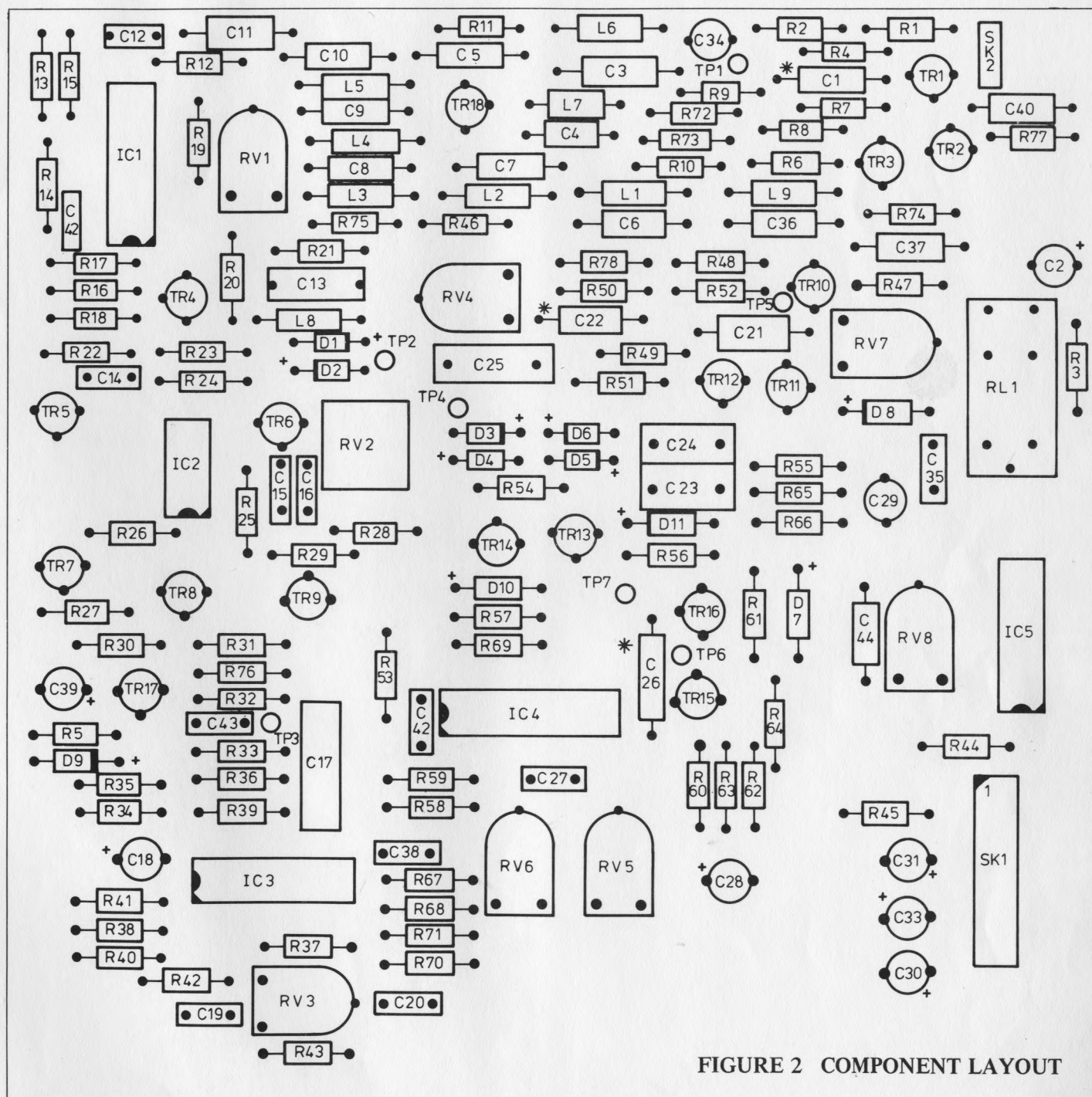


FIGURE 2 COMPONENT LAYOUT

* NOT FITTED.

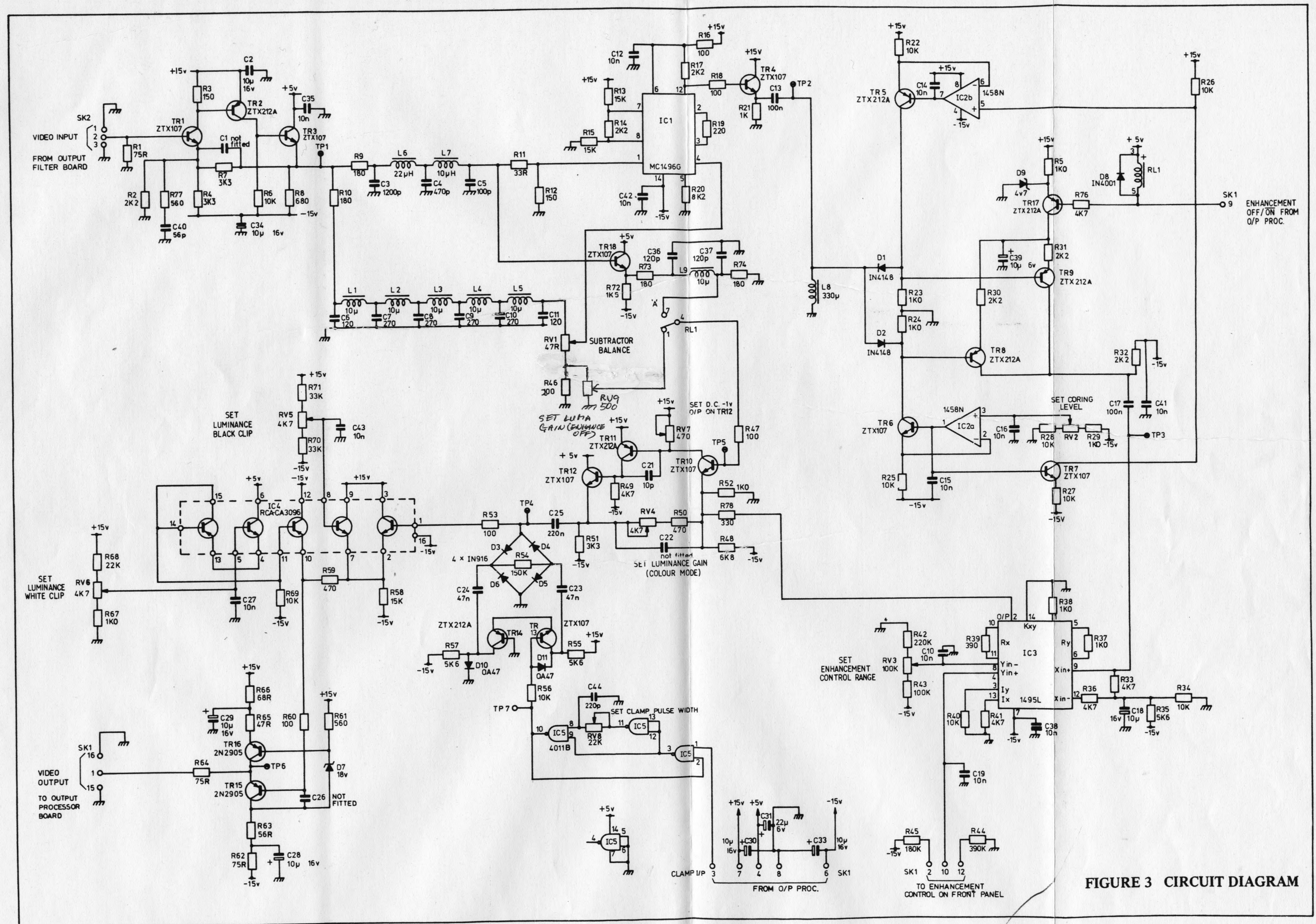


FIGURE 3 CIRCUIT DIAGRAM

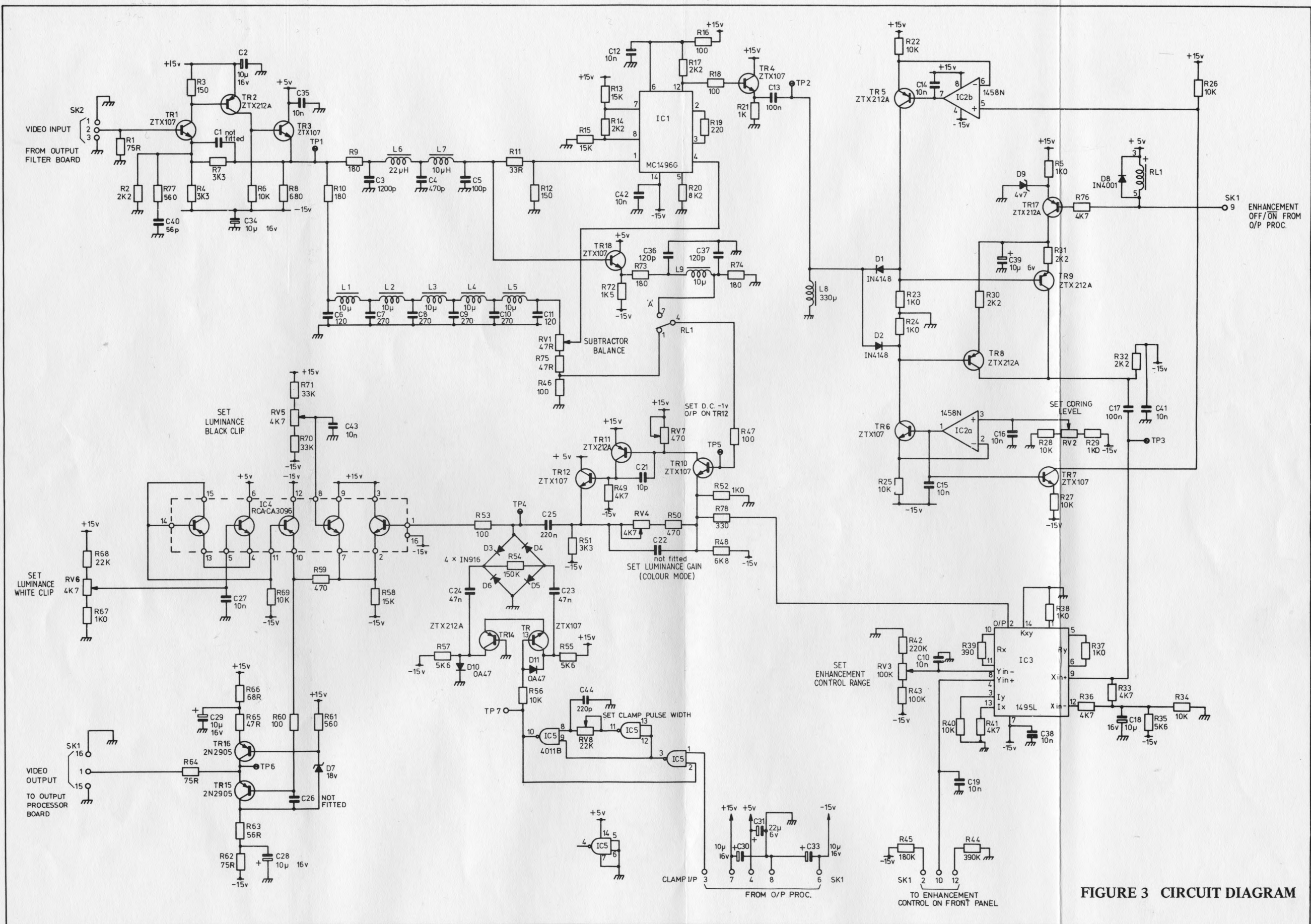


FIGURE 3 CIRCUIT DIAGRAM

OUTPUT
FILTER

**OUTPUT FILTER
IVC PCB GL209**

DESCRIPTION	1
ADJUSTMENTS	1
CONNECTIONS	1
TEST POINTS	1
COMPONENT SCHEDULE	2

FIGURE 1 COMPONENT LAYOUT

(NB The circuit diagram for this card is included on the circuit diagram for the Output Processor card)

OUTPUT FILTER IVC PCB GL209

DESCRIPTION

The Output Filter card contains two low pass filters with their associated group delay correctors. The 3MHz LPF circuit is for colour operation, and the luminance signal from the Output Processor card is connected via PL6/4,3. The filtered output is taken from PL2/2,3 to the Enhancer card. The 5.5MHz LPF circuit is for monochrome operation, and the luminance signal from the Output Processor card is connected via PL6/2,1. The filtered output is taken from PL5/4,6 back to the Output Processor card.

The circuit diagram for the Output Filter card is included on the circuit diagram for the Output Processor card.

Links are provided for testing the filter and equalising circuits.

ADJUSTMENTS

There are no adjustments on this card. No attempt should be made to readjust these filters in the field.

CONNECTIONS

PL2 Luminance Output to Enhancer card

- 2 Luminance signal
- 3 Earth

PL5 Luminance output to Output Processor card

- 4 Luminance signal
- 6 Earth

PL6

Luminance input connections

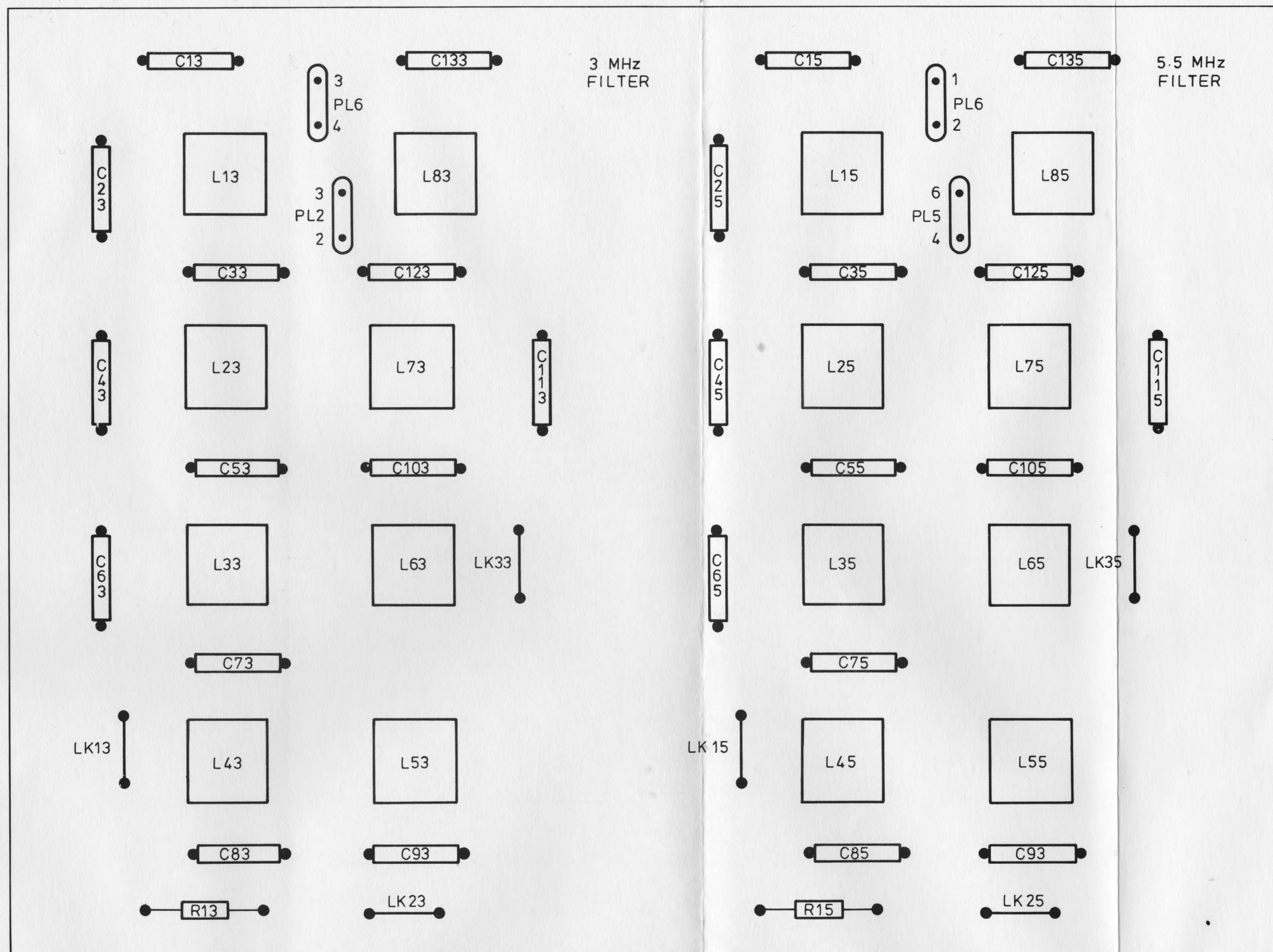
- 1 Earth
- 2 Luminance signal (monochrome)
- 3 Earth
- 4 Luminance signal (colour)

TEST POINTS

There are no test points on this card.

CIRCUIT REF.	DESCRIPTION	PART NO.
	3MHz FILTER	
C13		R530526
C23		R530090
C33		R531092
C43		R530250
C53		R530939
C63		R530631
C73		R530210
C83		R534114
C93		R530542
C103		R534140
C113		R531220
C123		R531220
C133		R533500
L13	Type Z	R600325
L23	Type Z	R600325
L33	Type S	R600318
L43	Type AD	R600329
L53	Type AD	R600329
L63	Type AA	R600326
L73	Type AB	R600327
L83	Type AC	R600328
R13	910 $\pm$ 2%, $\frac{1}{3}$ W	R441914
	5.5MHz FILTER	
C15		R530285
C25		R530049
C35		R530592
C45		R530136
C55		R530509
C65		R530342
C75		R530114
C85		R532230
C95		R530294

CIRCUIT REF.	DESCRIPTION	PART NO.
	5.5MHz FILTER (continued)	
C105		R532245
C115		R530661
C125		R530661
C135		R531898
L15	Type S	R600318
L25	Type S	R600318
L35	Type T	R600319
L45	Type Y	R600324
L55	Type Y	R600324
L65	Type V	R600321
L75	Type W	R600322
L85	Type X	R600323
R15	620 $\pm$ 2%, $\frac{1}{3}$ W	R441624



SPG

**SYNC PULSE GENERATOR
IVC PCB GL207**

INTRODUCTION	1
CIRCUIT DESCRIPTION	1
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CONNECTIONS	5
TEST POINTS	6
COMPONENT SCHEDULE	7

FIGURE 1	BLOCK DIAGRAM, MASTER OSCILLATOR WITH HORIZONTAL AND VERTICAL DIVIDERS
FIGURE 2	BLOCK DIAGRAM, LOCKING INPUT INTERFACES AND OUTPUT STAGES
FIGURE 3	BLOCK DIAGRAM, ADVANCED VTR LOCK CONTROL
FIGURE 4	COMPONENT LAYOUT
FIGURE 5	CIRCUIT DIAGRAM, SHEET 1
FIGURE 6	CIRCUIT DIAGRAM, SHEET 2

SYNC PULSE GENERATOR

IVC PCB GL207

INTRODUCTION

The Sync Pulse Generator (SPG) card contains a complete gen-lockable 625-50 sync pulse generator which supplies the required output pulses for all modes of operation for the TBC-2002.

For capstan servo, internal mode, the SPG derives all pulses from its own 8.866MHz temperature-compensated crystal oscillator (TCXO). The oscillator output is divided by two to produce PAL subcarrier frequency, and this is further divided down to $fH/4$ to phase-lock the 106MHz master oscillator loop.

For capstan servo, external video mode, the SPG master oscillator is phase-locked to horizontal syncs separated from an external video input. The subcarrier frequency is derived from a burst locked oscillator which is locked to the video signal. The vertical counter is reset by vertical syncs, and the ident signal is derived from the incoming swinging burst.

For capstan servo, external syncs mode, the SPG master oscillator is phase-locked to horizontal syncs separated from external composite sync pulses, and the vertical counter is reset by vertical syncs from these composite sync pulses. The subcarrier frequency and ident signals are also derived from the external reference inputs.

For non capstan servo mode, the master oscillator is phase-locked to vertical syncs derived from the OFF TAPE input to the TBC-2002. The subcarrier frequency is derived from the internal TCXO. The subcarrier and syncs are not correctly related.

In addition to the main SPG circuitry, the card also contains the output buffer stages for the rear panel pulse outputs and the drop-out detector circuitry.

CIRCUIT DESCRIPTION

Mode Selector Circuit

The required operating mode is determined by the controls on the front panel and the REFERENCE INPUTS on the rear panel.

The controls determine the state of the signals input to the SPG card via SK8. These signals are gated in IC27 and IC28 to provide the control signals for the subcarrier select circuit (IC1) and the master oscillator control circuits. They are also used to switch in the appropriate REFERENCE INPUT signal.

The COMP VIDEO or SUBCARR reference input from the rear panel is connected to the SPG card via SK5/15 and is input to one gate of dual FET, TR3. Current source TR2 is switched on by TR1 in capstan servo, external mode only, and allows the input signal to be amplified by a factor of 5 at the collector of TR4. The signal at the collector of TR4 is connected via R22 to the subcarrier selector IC1/4, and via R12 and C4 to the burst locked oscillator circuits.

The chroma components are removed by low pass filter L1, C119, C120, and the luminance components are applied to the base of TR6 via transmission gate IC2/3 which is enabled for external video mode. For external syncs mode, the COMP SYNCs reference input from the rear panel is input to the SPG card via SK5/13 and switched into transmission gate IC2/2 (enabled for external syncs mode) via TR7. The output of the transmission gate is applied to the base of TR6 via R54. The emitter of TR6 provides the input for the sync separator circuit.

Sync Separator

The signal at the emitter of TR6 is coupled via C29 to a diode bridge clamp comprising D13, D14, D15, D16. The signal is clipped by TR45 and the resultant sync signal is applied to IC40/4. The sync pulses are peak detected (TR47, TR48) and a voltage equal to half the sync amplitude is applied to IC40/3 via TR50. IC41 and TR49 form a start-up circuit which ensures correct operation.

The separated TTL level syncs at IC40/9 trigger monostable IC36/9 on the negative edge to produce the $38\mu\text{s}$ H SYNC pulses at IC36/5. Monostable IC36/2 is triggered on the positive edge to produce clamp pulses and burst gate pulses at the Q and $\bar{Q}$ outputs respectively. IC35/3 is clocked by H SYNC pulses from IC36/5 and reset by clamp pulses from IC36/13. The $\bar{Q}$ output at IC35/2 disables IC36/1 when it is high in order to ensure only one clamp pulse is generated for each horizontal period.

Field Pulse Detector

TR51, in conjunction with C97 and R190, forms a field pulse detector which triggers monostable IC37/2 approximately $15\mu\text{s}$ into the first broad pulse. The positive edge of the pulse at IC37/13 clocks IC35/11 whose D input receives the $38\mu\text{s}$ H SYNC pulses from IC36/12. The output on IC35/12 is a type 1 (even)/type 2 (odd) field indicator which produces a negative-going pulse at the start of a type 2 field. This pulse is used to load the vertical counter (IC10, IC11, IC12) in the capstan servo, external sync mode.

Temperature-Compensated Crystal Oscillator

For the capstan servo, internal sync mode, the $\overline{\text{INT/EXT}}$ signal on SK8/16 is low and TR20 is turned on. This connects +5V to the temperature-compensated crystal oscillator TCXO which operates at twice subcarrier frequency. The TTL level output from pin 1 clocks the divide-by-2 circuit IC31 to produce subcarrier frequency at IC31/9 which is low pass filtered to give a sine wave signal at the junction of L11 and R80. This sine wave is connected to the input of subcarrier selector (IC1/11) via C15 to provide the internal subcarrier signal for the mode select circuit. It is also fed to balanced modulators IC51 and IC52 via R92 to generate the fH/4 signal for the master oscillator control circuit.

The 0° subcarrier is connected to IC51/10 via R114, while L14, C63 and CV1 phase shift the subcarrier through 90° and feed it to IC52/10. The inputs on IC51/4 and IC52/4 are derived from the 25Hz squarewave from IC16/12. This is connected to low pass filter R122, R123, C56, C57, etc, and

the sine wave at IC55/7 is taken to IC51/4 via C70. It is also fed to a 90° phase shifter consisting of R125, R126, C58 and IC55/1 and connected to IC52/4 via C64.

The balanced modulator outputs are combined in transformer T2 and passed via a low pass filter to the input of comparator IC56. The frequency of the signal, monitored at TP4, is subcarrier frequency minus 25Hz. The TTL level output at IC56/9 is converted to a 12V swing by TR22 and clocks divide-by-227 circuit IC54. The output at IC54/15 is connected via R86 to the clock input of divide-by-5 circuit IC53/2. The output at IC53/12 is at fH/4 and is connected to the mode selector multiplexer IC46/12.

Master Oscillator Circuits

The master oscillator runs at a frequency of 106MHz (6810fH) and consists of FET oscillator TR25. The frequency is controlled by the tuned circuit comprising L15 and varactor diode D10, and the amplitude of oscillation is set by RV2.

The master oscillator is controlled by phase comparator IC47. The output currents from IC47/13 and 2 charge the oscillator loop filter circuits via D8, R129 and D9, R128. The appropriate loop filter circuit is selected by FET TR24, TR26 or TR56, depending on the operating mode. TR56 is switched on in the CAPSTAN SERVO mode; TR24 is the NON CS track slow mode, and TR26 in the NON CS track fast mode. The inputs to the phase comparator are selected by multiplexer IC46.

For capstan servo internal mode, IC46/10 and 9 are both low and therefore X_o and Y_o are selected for outputs X_c and Y_c respectively. The input at X_o is the fH/4 signal from TCXO; the input at Y_o is also fH/4 and is derived from IC44 which is clocked by IC42/11. This signal is determined by the COL/MONO signal input on SK8/13 and the horizontal blanking signal from IC22/2.

For capstan servo, external mode, IC46/10 is low and IC46/9 is high so that X_c and Y_c select inputs X_1 and Y_1 respectively. X_1 is the separated horizontal syncs from the SPG sync separator, and Y_1 is derived from the $\bar{Q}$ output (pin 12) of monostable IC87. This monostable is triggered from IC42/11, and the period of the $\bar{Q}$ pulse is determined by the front panel SYSTEM H-PHASE control by means of operational amplifier IC48 and current source TR23.

For non capstan servo mode, X_c and Y_c select X_3 and Y_3 respectively. X_3 is a separated vertical pulse derived from the OFF TAPE V signal from the Input Processor card, and Y_3 is the vertical pulse REF V from the SPG vertical divider. These pulses are routed to SK1/12 and 14 respectively via the Store card.

The oscillator output is coupled via C78 to the two halves of IC50 and IC49. IC50/10 forms a divide-by-2 circuit, and its output, on pin 14, provides the 53MHz pulsetrain for the Quad Dub card via SK4/2. IC50/7 and IC49 form a divide-by-5 circuit and their outputs are taken to a divide-by-3 circuit (IC45) via ECL to TTL convertor TR27 and TR28. The 454fH (7.09MHz) pulsetrain from IC45/7 is taken to the Store card via SK1/11, and that from IC45/5 provides the clock pulses for the SPG horizontal divider.

Burst Locked Oscillator

The signal at the collector of TR4 is coupled via R12 and C4 to the source of FET TR58 which acts as a burst gate. 5V burst gate signals from the sync separator (IC34/8) are converted to 12V level by TR5 and connected to the gate of TR58. The gated burst at the drain of TR58 is transformer-coupled by T1 to the input of burst locked oscillator IC5/5. The burst locked subcarrier output is from IC5/4 and is taken to the subcarrier select circuit (IC1/1). The colour kill output is from IC5/7.

When a signal with a PAL burst is present, IC5/7 has a high impedance which turns on TR10 and lights up the green LED above the COMP VIDEO/SYNCS switch on the front panel. RV8 sets the threshold level for the colour killer in IC5. IC14/3 is clocked by H SYNCS pulses from the sync separator to produce IDENT squarewave at IC14/1. This is coupled to IC5/8 via R23 and C18.

Horizontal and Vertical Dividers

The 7.09MHz clock pulses from the divide-by-3 counter in the master oscillator circuit (IC45/5) are applied to the horizontal divide-by-454 counter comprising IC23, IC24 and IC26. The load pulse $\bar{L}$ at the output of IC25/8 loads the counter with a count of 58 and the counter is clocked down to a terminal count of 511. The 9-bit output forms the address to PROM IC20 which contains the horizontal sync pulse timing information. The 8-bit output from IC20 is latched by IC21, IC22, and each horizontal rate pulsetrain is available at their Q and $\bar{Q}$ outputs.

The 2fH pulses from output latch IC21/3 clock the vertical 625 counter consisting of IC10, IC11, IC12. At a count of 624, IC13/13 goes low and clears the counter via differentiator C48 and R66. The vertical counter may be loaded to a count determined by the parallel inputs (P1, P2, P3, P4) on IC10, IC11, IC12 by means of the load pulse $\bar{L}$ on pin 9 of each IC. This $\bar{L}$ input is only used in the capstan servo, external syncs mode to vertically phase the output syncs to the reference syncs.

Of the 10-bit output from the vertical counter, the lower 8 bits and the 10th bit form the address to PROM IC7 which contains the vertical sync pulse timing information. The 8-bit output from IC7 is latched by IC8, IC9 which are clocked by the 2fH pulses from IC21/2. The ADV'D 2fH pulses from IC21/15 turn on transistor TR17 which connects the +5V supply to IC7. This ensures IC7 is only powered for 2 μ s in every 32 μ s, and that it is in fact powered just before the output latches (IC8, IC9) are clocked.

In order that IC7, which is a 512 word PROM, may be used in conjunction with a 625 address counter, the output latch clock pulses are inhibited by a low on IC15/5 when bit 9 from the vertical counter (IC10/4) is high. This removes 256 clock pulses during that part of the active field when no output sync transitions are required.

The 2nd, 3rd and 4th bits of the parallel input to the vertical counter (IC12/4, 5 and 6) are adjustable by link LK9. This allows the output vertical phase with respect to the locking reference to be varied in increments of one horizontal period.

The horizontal rate pulsetrains from IC21, IC22, and the vertical rate pulsetrains from IC8, IC9 are used to produce the six standard INTERNAL SYNC GEN OUTPUTS from the rear panel of the TBC-2002 (i.e. COMP SYNC, COMP BLK, BURST GATE, PAL IDENT, H DRIVE, V DRIVE).

Sync Pulse Combining Circuits

The horizontal drive signal, HORIZ DRIVE, from IC22/14, and the vertical drive signal, VERT DRIVE, from IC8/14 are switched into their respective output stages by TR32 and TR33.

Broad pulses (BRDS), equalising pulses (EQ) and horizontal syncs (HS) from IC21 and IC22 are gated with their respective BRDS, EQ and EQ gating pulses from IC8 and IC9 to produce MIXED SYNCS pulses at IC17/6. This is taken to the Output Processor card via SK2/2, and is also switched into the composite syncs output stage by TR29.

The true horizontal syncs pulsetrain (HS) from IC22/10 is used as the READ H signal for the optional Quad Dub card (via SK4/5) and the Output Processor card (via SK2/4). It is also inverted at IC19/6 to provide the READ H signal for the Store card via SK1/8.

Normal or narrow (short) vertical blanking pulses are selected by link LK8 and gated with the horizontal blanking signal (H BLK) to produce the MIXED BLANKING signal at IC15/3. This is switched into the composite blanking output stage by TR30.

The horizontal blanking signal is also input to IC16/9 and is clocked by the normal vertical blank-

ing signal on IC16/11 to produce a 25Hz square-wave. The output from IC16/13 is used as the ODD/EVEN signal for the Store card (via SK1/15), and also clocks IC16/3 to produce a 12.5Hz square-wave at IC16/1 and 2. This selects either vertical burst gate VBG(1) or VBG(2) from IC9/7 or 15. The selected signal is gated with the horizontal burst gate signal, HBG, from IC22/7 to produce the correct BRUCH blanked BURST GATE at IC19/10. This BURST GATE signal is taken to the Output Processor card via SK2/14, and is also switched into the burst gate output stage by TR31.

Horizontal syncs from IC22/11 clock the divide-by-2 circuit IC32 to produce a 7.8Hz square-wave IDENT signal. A series of links allows the phase and type of IDENT pulse to be selected. For a squarewave IDENT pulse, link LK6 is in position A or C to select the true or inverted 7.8kHz squarewave. For a DIN IDENT pulse, link LK6 is in position B and LK4 selects the true or inverted 7.8kHz squarewave which is fed to a pulse shaping circuit comprising C14, R204. The required signal is switched into the PAL IDENT output stage by TR34. Link LK5 selects the correct phase of the IDENT signal, whether squarewave or DIN, for the Output Processor card (via SK2/3).

Internal Sync Gen Output Stages

The six standard pulsetrains derived from the horizontal and vertical divider circuits (MIXED SYNCs, MIXED BLANKING, BURST GATE, HORIZ DRIVE, VERT DRIVE, IDENT) are each applied to a filter circuit to produce a controlled risetime, and drive a 75 ohm output stage. The 2.5V reference for the filter circuits is derived from the +5V rail via TR36, and the -0.7V reference for the 75 ohm output stages is obtained from D11, R153 and C87. The resultant outputs (COMP SYNC, COMP BLNK, BURST GATE, H DRIVE, V DRIVE, PAL IDENT) are connected to rear panel BNC connectors.

The VTR SYNCs signal input from the Store card via SK1/9 is also applied to a filter and 75 ohm output drive stage to provide the VTR LOCK output signal. With the PLAY BACK/BYPASS/RECORD switch on the front panel in the PLAY BACK position, relay RL1 is de-energised and the VTR LOCK signal from the output stage is connected to the rear panel BNC connector. With the switch in the RECORD position, relay RL1 is energised and switches the RECORD VIDEO IN input on the rear panel through to the VTR LOCK BNC connector.

Subcarrier Select Circuit

The circuit selects one of four subcarrier

signals. The external subcarrier is derived either from the COMP VIDEO or SUBCARR reference signal input via SK5/15 and switched into transmission gate IC1/4 by TR4, or from the optional Quad Dub card input via SK3/2 to IC1/8 or from the burst locked oscillator (IC5/4) and input to IC1/1. The internal subcarrier is derived from the TCXO and input to IC1/11.

The selected subcarrier is switched into the coarse phase shifter circuit by TR11. This circuit includes three delay lines (C24, L3; C26, L4; C27, L5) which are selected by IC6 under the control of the 4-position SYSTEM PHASE control on the front panel. (The first position bypasses the delay lines). The subcarrier signal is then switched via TR12 into the fine phase shifter circuit comprising CV2, C33, L6, D3, D4. This circuit is adjusted by the left-hand SYSTEM PHASE control on the front panel to allow the output video to be in phase with the reference. TR13 switches the subcarrier into a limiter (C7, CV3, D6, D7) from where it is connected to the output stage via TR14.

From the emitter of TR14 the subcarrier is fed to the Output Processor card via SK2/1 and to the Direct Record card (if fitted) via SK7/2. It is also "sliced" by the emitter-coupled pair TR15, TR16 and applied to the bandpass filter circuit L9, C46, C47, L8. The resulting sine wave is buffered by TR18 and TR19 and taken to the SUBCARR output BNC connector via SK6/1.

Drop-Out Compensator Detector Circuit

The DOC RF signal from the VTR demodulator is input via the DOC IN connector on the rear panel and enters the SPG card via SK5/6. It is passed through a buffer amplifier circuit comprising TR54 and TR55, and input to phase comparator IC3/11. The buffered RF signal is also rectified by D25 and D26 so that a signal representing the envelope is obtained at IC3/12. A time constant for detection is set by C106, C107, R226, R228 and RV7 (which adjusts the threshold).

The resultant RF pulses at IC3/9 fire the retriggerable monostable IC4 such that IC4/8 will normally stay high and will go low during drop-out. D27 and C108 give a fast pull down at the start of the drop-out, and R228, C108 give a slow rise time at the end of the drop-out. The drop-out pulses are taken to IC3/2 via LK2 where they are compared with 2.5V at IC3/1 to give TTL level pulses at IC3/4. These pulses are combined in IC57 with the field DOC BLANKING pulses from the vertical divider circuit (IC8/7) and the DOC signal on SK8/14 input from the DOC ON/OFF switch on the front panel. The output on IC57/8 is taken to the Store card via SK1/16. Link LK1 allows the RF input.

Link LK1 allows the RF input to be terminated in 75 ohms if required, and link LK2 allows a DOC pulse to be used for the DOC input. Normally the DOC input is RF and LK2 is in position B. If the input is a TTL level pulse, LK2 is moved to position A to bypass the RF detector circuit.

ADJUSTMENTS

CV1,— Adjust the balance on the 25Hz subcarrier RV4, modulators. Each is adjusted in turn for RV5, minimum twitter on the subcarrier output RV6 as monitored on TP4 or IC56/3.

CV2 — Peaks the subcarrier frequency tuned circuit in the fine phase shifter circuit. With the left-hand SYSTEM PHASE control on the front panel set at mid range, adjust CV2 is adjusted for a maximum amplitude at SK7/2.

CV3 — Peaks the subcarrier frequency tuned circuit in the subcarrier limiter circuit. After adjusting CV2, CV3 is adjusted for maximum limiting at SK7/2.

CV4 — Adjusts the free running frequency of the burst locked oscillator. With CAPSTAN SERVO, EXT and COMP VIDEO selected on the front panel, and the video lock input on the rear panel disconnected, adjust CV4 to give a frequency of 4.43361875MHz at the subcarrier output on the rear panel.

R274 — The value of this resistor sets the amplitude of the PAL IDENT output on the rear panel. It is normally 560 ohms for 2V squarewave, and should be changed to 1k2 ohms for 1V (i.e. DIN) squarewave.

RV1 — Adjusts the output voltage of the master oscillator. Set to give -1.25V at TP2.

RV2 — Adjusts oscillation level of master oscillator (106MHz). Set for reliable oscillator operation. Normally at minimum resistance fully clockwise.

RV3 — Adjusts the output picture timing relative to locking inputs in colour mode. Set so that the picture timing at the output remains the same when switching from colour to monochrome.

RV7 — Adjusts the drop-out compensator threshold level.

RV8 — Adjusts the threshold of the colour lock LED on the front panel. Set so that the LED extinguishes.

LK1 — Terminates RF DOC input in 75 ohms.

LK2 — Selects RF or pulse DOC input.

Position A — Pulse

Position B — RF

LK3 — Selects IDENT phase for external sync mode. Note that changing this link also means changing link LK7 accordingly.

LK4 — Selects the polarity of the DIN IDENT pulse.

LK5 — Selects polarity of the IDENT pulse to the Output Processor. Normally in position A.

LK6 — Selects IDENT pulse for output from rear panel.

Position A — Squarewave

Position B — DIN pulse

Position C — Inverted squarewave

LK7 — Selects IDENT phase for external video mode.

LK8 — Selects normal or narrow field blanking.

Position A — Normal

Position B — Narrow

CONNECTIONS

SK1 Store card connections

8	READ H
9	VTR SYNC
10	REF V
11	454fH
12	OFF TAPE V
13	V BURST BLK
14	REF V
15	ODD/EVEN
16	DOC control

SK2 Output Processor card connections

1	Subcarrier
2	MIXED SYNC
3	IDENT
4	READ H
14	BURST GATE

SK2 Output Processor card connections
(continued)

- 15 Ground (Subcarrier)
- 16 Ground (Subcarrier)

SK3 Power connections

- 2 +15V
- 3 Ground
- 4,5,6 +5V
- 7,8 Ground
- 10 Ground
- 11,12 -5.2V
- 13,14, Ground
- 15 -15V

SK4 Quad Dub card connections

- 1 Ground (53MHz)
- 2 53MHz
- 3 Ground (53MHz)
- 5 READ H
- 6 0V
- 7 -15V
- 8 -5.2V
- 9 +5V
- 10 +15V

SK5 Rear panel inputs

- 1 Ground (RECORD VIDEO IN)
- 2 RECORD VIDEO IN
- 3 Ground (PAL IDENT)
- 4 PAL IDENT
- 5 Ground (DOC IN)
- 6 DOC IN
- 7 +12V
- 8 +5V
- 13 COMP SYNCs
- 14 Ground (COMP SYNCs)
- 15 COMP VIDEO/SUBCARR
- 16 Ground (COMP VIDEO/SUBCARR)

SK6 Rear panel outputs

- 1 SUBCARR
- 2 Ground (SUBCARR)
- 3 PAL IDENT
- 4 Ground (PAL IDENT)
- 5 V DRIVE
- 6 Ground (V DRIVE)
- 7 H DRIVE
- 8 Ground (H DRIVE)
- 9 BURST GATE
- 10 Ground (BURST GATE)
- 11 COMP BLNK

SK6 Rear panel outputs (continued)

- 12 Ground (COMP BLNK)
- 13 COMP SYNCs
- 14 Ground (COMP SYNCs)
- 15 VTR LOCK
- 16 Ground (VTR LOCK)

SK7 Direct Record card connections

- 1 Ground (SUBCARRIER)
- 2 SUBCARRIER
- 3 Ground (SUBCARRIER)

SK8 Front panel connections

- 1 TRACK FAST/SLOW
- 2 PAL COLOUR LED
- 3 +5V, PAL COLOUR LED
- 4 SYSTEM SC PHASE, coarse, 90°
- 5 SYSTEM SC PHASE, coarse, 270°
- 6 SYSTEM SC PHASE, coarse, 0°
- 7 SYSTEM SC PHASE, coarse, 180°
- 8 Ground, SYSTEM SC PHASE, fine
- 9 SYSTEM SC PHASE, fine control
- 10 +15V, SYSTEM SC PHASE, fine
- 11 CAPSTAN SERVO/NON CS
- 12 COMP VIDEO/SYNCs
- 13 COL/MONO
- 14 DOC ON/OFF
- 15 QUAD DUB/NORM
- 16 INT/EXT

SK9 Front panel connections

- 1 RECORD
- 2 Ground (RECORD)
- 3 Ground (SYSTEM H PHASE)
- 4 SYSTEM H PHASE control
- 5 +15V (SYSTEM H PHASE)

SK10 Quad Dub card connections

- 1 Ground (SUBCARRIER)
- 2 SUBCARRIER
- 3 QUAD DUB/NORM

TEST POINTS

- TP1 Master oscillator control loop, phase comparator output
- TP2 Master oscillator frequency
- TP3 Earth
- TP4 Subcarrier frequency minus 25Hz
- TP5 21.28MHz frequency
- TP6 Earth
- TP7 Burst locked oscillator frequency

CIRCUIT REF.	DESCRIPTION	PART NO.
	CAPACITORS	
C1	220nF $\pm 10\%$, 63V	R522245
C2	10nF, 25V	R501033
C3	10nF, 25V	R501033
C4	10nF, 25V	R501033
C5	10 μ F, 16V	R541062
C6	22 μ F, 6.3V	R542261
C7	10 μ F, 16V	R541062
C8	39pF $\pm 2\frac{1}{2}\%$, 63V	R513905
C9	120pF $\pm 2\frac{1}{2}\%$, 63V	R511215
C10	10nF, 25V	R501033
C11	10nF, 25V	R501033
C12	Not fitted	—
C13	10nF, 25V	R501033
C14	10nF, 25V	R501033
C15	10nF, 25V	R501033
C16	10nF, 25V	R501033
C17	10nF, 25V	R501033
C18	220nF $\pm 10\%$, 63V	R522245
C19	220nF $\pm 10\%$, 63V	R522245
C20	10 μ F, 16V	R541062
C21	220nF $\pm 10\%$, 63V	R522245
C22	220nF $\pm 10\%$, 63V	R522245
C23	10nF, 25V	R501033
C24	82pF $\pm 2\frac{1}{2}\%$, 63V	R518205
C25	220pF $\pm 2\frac{1}{2}\%$, 63V	R512215
C26	150pF $\pm 2\frac{1}{2}\%$, 63V	R511515
C27	150pF $\pm 2\frac{1}{2}\%$, 63V	R511515
C28	82pF $\pm 2\frac{1}{2}\%$, 62V	R518205
C29	220nF, 63V	R522245
C30	10nF, 25V	R501033
C31	10nF, 25V	R501033
C32	Not fitted	—
C33	10pF, 63V	R511005
C34	10nF, 25V	R501033

CIRCUIT REF.	DESCRIPTION	PART NO.
	CAPACITORS (continued)	
C35	10nF, 25V	R501033
C36	10nF, 25V	R501033
C37	10nF, 25V	R501033
C38	10nF, 25V	R501033
C40	Not fitted	—
C41	10nF, 25V	R501033
C42	10nF, 25V	R501033
C43	220nF, 63V	R522245
C45	10nF, 25V	R501033
C46	27pF $\pm 2\frac{1}{2}\%$, 63V	R512705
C47	270pF $\pm 2\frac{1}{2}\%$, 63V	R512715
C48	100pF $\pm 2\frac{1}{2}\%$, 63V	R511015
C49	22 μ F, 6.3V	R542261
C50	100nF $\pm 10\%$, 100V	R521046
C51	10nF, 25V	R501133
C52	22 μ F, 6.3V	R542261
C53	220pF $\pm 2\frac{1}{2}\%$, 63V	R512215
C54	220pF $\pm 2\frac{1}{2}\%$, 63V	R512215
C55	10 μ F, 16V	R541062
C56	47nF $\pm 10\%$, 100V	R524736
C57	100nF $\pm 10\%$, 100V	R521046
C58	100nF $\pm 10\%$, 100V	R521046
C59	10nF, 25V	R501033
C60	68pF $\pm 2\frac{1}{2}\%$, 63V	R516805
C61	22pF $\pm 2\frac{1}{2}\%$, 63V	R512205
C62	Not fitted	—
C63	68pF $\pm 2\frac{1}{2}\%$, 63V	R516805
C64	10 μ F, 16V	R541062
C65	10 μ F, 16V	R541062
C66	10nF, 25V	R501033
C67	10nF, 25V	R501033
C68	10nF, 25V	R501033
C69	10 μ F, 16V	R541062
C70	10 μ F, 16V	R541062

CIRCUIT REF.	DESCRIPTION	PART NO.
	CAPACITORS (continued)	
C71	1500pF $\pm 2\frac{1}{2}\%$, 63V	R511525
C72	100nF $\pm 10\%$, 100V	R521046
C73	100nF $\pm 10\%$, 100V	R521046
C74	1000nF, 35V	R541054
C75	15pF $\pm 2\frac{1}{2}\%$, 63V	R511505
C76	100pF $\pm 2\frac{1}{2}\%$, 63V	R511015
C77	10nF, 25V	R501033
C78	100pF $\pm 2\frac{1}{2}\%$, 63V	R511015
C79	10nF, 25V	R501033
C81	10nF, 25V	R501033
C82	470pF $\pm 2\frac{1}{2}\%$, 63V	R514715
C83	220pF $\pm 2\frac{1}{2}\%$, 63V	R512215
C84	47pF $\pm 2\frac{1}{2}\%$, 63V	R514705
C85	10 μ F, 16V	R541062
C86	10 μ F, 16V	R541062
C87	22 μ F, 6.3V	R542261
C88	22 μ F, 6.3V	R542261
C89	47nF $\pm 10\%$, 100V	R524736
C90	47nF $\pm 10\%$, 100V	R524736
C91	220pF $\pm 2\frac{1}{2}\%$, 63V	R512215
C92	47pF $\pm 2\frac{1}{2}\%$, 63V	R514705
C93	470nF $\pm 10\%$, 63V	R524745
C94	1000pF $\pm 2\frac{1}{2}\%$, 63V	R511025
C95	10nF, 25V	R501033
C96	10nF, 25V	R501033
C97	10nF $\pm 10\%$, 100V	R521036
C98	22 μ F, 6.3V	R542261
C99	4700pF $\pm 2\frac{1}{2}\%$, 63V	R514725
C100	100nF $\pm 10\%$, 100V	R521046
C101	Not fitted	—
C102	470pF $\pm 2\frac{1}{2}\%$, 63V	R514715
C103	100nF $\pm 10\%$, 100V	R521046
C104	10nF, 25V	R501033
C105	10nF, 25V	R501033

CIRCUIT REF.	DESCRIPTION	PART NO.
	CAPACITORS (continued)	
C106	10nF, 25V	R501033
C107	470nF $\pm 10\%$, 63V	R524745
C108	1200pF $\pm 2\frac{1}{2}\%$, 63V	R511225
C109	10nF, 25V	R501033
C110	220pF $\pm 2\frac{1}{2}\%$, 63V	R512215
C111	330pF $\pm 2\frac{1}{2}\%$, 63V	R513315
C112	330pF $\pm 2\frac{1}{2}\%$, 63V	R513315
C113	470pF $\pm 2\frac{1}{2}\%$, 63V	R514715
C114	470pF $\pm 2\frac{1}{2}\%$, 63V	R514715
C115	10 μ F, 16V	R541062
C116	22 μ F, 6.3V	R542261
C117	22 μ F, 6.3V	R542261
C118	10 μ F, 16V	R541062
C119	150pF $\pm 2\frac{1}{2}\%$, 63V	R511515
C120	470pF $\pm 2\frac{1}{2}\%$, 63V	R514715
C121	33pF $\pm 2\frac{1}{2}\%$, 63V	R513305
C122	10 μ F, 16V	R541062
C123	470nF $\pm 10\%$, 63V	R524745
C124	47nF $\pm 10\%$, 100V	R524736
C125	15nF $\pm 10\%$, 100V	R521536
C126	56pF $\pm 2\frac{1}{2}\%$, 63V	R515605
C127	10nF, 25V	R501033
C128	Not fitted	—
C129	10 μ F, 16V	R541062
C130	10nF, 25V	R501033
C131	220pF $\pm 2\frac{1}{2}\%$, 63V	R512215
C132	47pF $\pm 2\frac{1}{2}\%$, 63V	R514705
C133	220pF $\pm 2\frac{1}{2}\%$, 63V	R512215
C134	47pF $\pm 2\frac{1}{2}\%$, 63V	R514705
C135	220pF $\pm 2\frac{1}{2}\%$, 63V	R512215
C136	47pF $\pm 2\frac{1}{2}\%$, 63V	R514705
C137	220pF $\pm 2\frac{1}{2}\%$, 63V	R512215
C138	47pF $\pm 2\frac{1}{2}\%$, 63V	R514705
C139	220pF $\pm 2\frac{1}{2}\%$, 63V	R512215

CIRCUIT REF.	DESCRIPTION	PART NO.
	CAPACITORS (continued)	
C140	47pF $\pm 2\frac{1}{2}\%$, 63V	R514705
C141	220pF $\pm 2\frac{1}{2}\%$, 63V	R512215
C142	47pF $\pm 2\frac{1}{2}\%$, 63V	R514705
C143 – C149	10 μ F, 16V	R541062
C150 – C156	18pF, 25V	R501803
C157 – C163	10 μ F, 16V	R541062
C164	47 μ F, 6.3V	R544761
C165	10 μ F, 16V	R541062
C166	10 μ F, 16V	R541062
C167	47 μ F, 6.3V	R544761
C168	10 μ F, 16V	R541062
C169	1000nF, 35V	R541054
C170 – C201	10nF, 25V	R501033
C202	Not fitted	—
C203 – C205	10nF, 25V	R501033
CV1 – CV4	2 – 22pF, variable	R591222
	DIODES	
D1	1N916	R350916
D2	1N916	R350916
D3	BA102B	R372102
D4	BA102B	R372102
D5	1N4148	R354148
D6	1N916	R350916
D7	1N916	R350916
D8	1N4148	R354148
D9	1N4148	R354148
D10	BA102B	R372102
D11	1N4148	R354148
D12	1N1001 or 1N4003	R351001 R354003
D13	1N916	R350916
D14	1N916	R350916
D15	1N916	R350916
D16	1N916	R530916

CIRCUIT REF.	DESCRIPTION	PART NO.
	DIODES (continued)	
D17	OA47	R385047
D18	OA47	R385047
D19	1N4148	R354148
D20	1N4148	R354148
D21	1N4148	R354148
D22	1N4148	R354148
D23	OA47	R385047
D24	1N4148	R354148
D25	OA47	R385047
D26	OA47	R385047
D27	1N4148	R354148
D28	OA47	R385047
D29	1N4148	R354148
D30	1N4148	R354148
D31	1N4148	R354148
D32	1N4148	R354148
D33	Not fitted	—
D34	Not fitted	—
D35	1N4148	R354148
	INTEGRATED CIRCUITS	
IC1	4066B	R261066
IC2	4066B	R261066
IC3	75107	R289107
IC4	74LSI22	R240122
IC5	TBA540	R280540
IC6	4066B	R261066
IC7	93448	R219448
IC8	14175B	R262175
IC9	14175B	R262175
IC10	14161B	R262161
IC11	14161B	R262161
IC12	14161B	R262161
IC13	4012B	R261012
IC14	4013B	R261013

CIRCUIT REF.	DESCRIPTION	PART NO.
INTEGRATED CIRCUITS (continued)		
IC15	4011B	R261011
IC16	4013B	R261013
IC17	4023B	R261023
IC18	4001B	R261001
IC19	4025B	R261025
IC20	93448	R219448
IC21	75LS175	R240175
IC22	74LS175	R240175
IC23	74LS161	R240161
IC24	74LS161	R240161
IC25	74LS10	R240010
IC26	74LS112	R240112
IC27	4002B	R261002
IC28	4002B	R261002
IC29	4069B	R261069
IC30	4011B	R261011
IC31	74LS112	R240112
IC32	4013B	R261013
IC33	4001B	R261001
IC34	74LS40	R240040
IC35	4013B	R261013
IC36	74LS221	R240221
IC37	74LS221	R240221
IC38	4013B	R261013
IC39	4023B	R261023
IC40	NE529N	R280529
IC41	741N-8	R280741
IC42	4011B	R261011
IC43	4002B	R261002
IC44	4013B	R261013
IC45	74LS112	R240112
IC46	4052B	R261052
IC47	4013B	R261013
IC48	741N-8	R280741

CIRCUIT REF.	DESCRIPTION	PART NO.
INTEGRATED CIRCUITS (continued)		
IC49	10131	R250131
IC50	10131	R250131
IC51	MC1496P	R281496
IC52	MC1496P	R281496
IC53	14161B	
IC54	14569B	
IC55	1458N-8	R281458
IC56	710N	R280710
IC57	74LS30	R240030
INDUCTORS		
L1	22 μ H	R620223
L3	22 μ H	R620223
L4	22 μ H	R620223
L5	22 μ H	R620223
L6	22 μ H	R620223
L7	47 μ H	R620473
L8	4.7 μ H	R620472
L9	47 μ H	R620473
L10	Type E	R600004
L11	10 μ H	R620103
L12	33 μ H	R620333
L14	15 μ H	R620153
L15	Type D	R600003
L16	1 μ H	R620013
L17	Not fitted	—
L18	Not fitted	—
L19 – L25	33 μ H	R620333
OSCILLATORS		
TCXO	8.866MHz	R691308
X1	4.433MHz	R695443
RELAY		
RL1	6V coil, 2-pole	R790062
RESISTORS		
R1	220 $\pm$ 5%, $\frac{1}{3}$ W	R401224

CIRCUIT REF.	DESCRIPTION	PART NO.
	RESISTORS (continued)	
R2	4k7 $\pm 5\%$, $\frac{1}{3}$ W	R401475
R3	18k $\pm 5\%$, $\frac{1}{3}$ W	R401186
R4	6k8 $\pm 5\%$, $\frac{1}{3}$ W	R401685
R5	Not fitted	
R6	220 $\pm 5\%$, $\frac{1}{3}$ W	R401224
R7	100 $\pm 5\%$, $\frac{1}{3}$ W	R401104
R8	390 $\pm 5\%$, $\frac{1}{3}$ W	R401394
R9	100 $\pm 5\%$, $\frac{1}{3}$ W	R401104
R10	1k0 $\pm 5\%$, $\frac{1}{3}$ W	R401105
R11	1k5 $\pm 5\%$, $\frac{1}{3}$ W	R401155
R12	10R $\pm 5\%$, $\frac{1}{3}$ W	R401103
R13	100k $\pm 5\%$, $\frac{1}{3}$ W	R401107
R14	6k8 $\pm 5\%$, $\frac{1}{3}$ W	R401185
R15	220 $\pm 5\%$, $\frac{1}{3}$ W	R401224
R16	10k $\pm 5\%$, $\frac{1}{3}$ W	R401106
R17	47R $\pm 5\%$, $\frac{1}{3}$ W	R401473
R18	2k2 $\pm 5\%$, $\frac{1}{3}$ W	R401225
R19	1k0 $\pm 5\%$, $\frac{1}{3}$ W	R401105
R20	27k $\pm 5\%$, $\frac{1}{3}$ W	R401276
R21	3k3 $\pm 5\%$, $\frac{1}{3}$ W	R401335
R22	1k0 $\pm 5\%$, $\frac{1}{3}$ W	R401105
R23	3k3 $\pm 5\%$, $\frac{1}{3}$ W	R401335
R24	22k $\pm 5\%$, $\frac{1}{3}$ W	R401226
R25	330 $\pm 5\%$, $\frac{1}{3}$ W	R401334
R26	Not fitted	
R27	47k $\pm 5\%$, $\frac{1}{3}$ W	R401476
R28	220 $\pm 5\%$, $\frac{1}{3}$ W	R401224
R29	10k $\pm 5\%$, $\frac{1}{3}$ W	R401106
R30	270 $\pm 5\%$, $\frac{1}{3}$ W	R401274
R31	10k $\pm 5\%$, $\frac{1}{3}$ W	R401106
R32	1k0 $\pm 5\%$, $\frac{1}{3}$ W	R401105
R33	1k0 $\pm 5\%$, $\frac{1}{3}$ W	R401105
R34	100k $\pm 5\%$, $\frac{1}{3}$ W	R401107
R35	100k $\pm 5\%$, $\frac{1}{3}$ W	R401107

CIRCUIT REF.	DESCRIPTION	PART NO.
	RESISTORS (continued)	
R36	100k $\pm 5\%$, $\frac{1}{3}$ W	R401107
R37	100k $\pm 5\%$, $\frac{1}{3}$ W	R401107
R38	100 $\pm 5\%$, $\frac{1}{3}$ W	R401104
R39	470 $\pm 5\%$, $\frac{1}{3}$ W	R401474
R40	47k $\pm 5\%$, $\frac{1}{3}$ W	R401476
R41	3k9 $\pm 5\%$, $\frac{1}{3}$ W	R401395
R42	1k0 $\pm 5\%$, $\frac{1}{3}$ W	R401105
R43	100 $\pm 5\%$, $\frac{1}{3}$ W	R401104
R44	100k $\pm 5\%$, $\frac{1}{3}$ W	R401107
R45	47k $\pm 5\%$, $\frac{1}{3}$ W	R401476
R46	5k6 $\pm 5\%$, $\frac{1}{3}$ W	R401565
R47	820 $\pm 5\%$, $\frac{1}{3}$ W	R401824
R48	100 $\pm 5\%$, $\frac{1}{3}$ W	R401104
R49	22k $\pm 5\%$, $\frac{1}{3}$ W	R401226
R50	100 $\pm 5\%$, $\frac{1}{3}$ W	R401104
R51	470 $\pm 5\%$, $\frac{1}{3}$ W	R401474
R52	8k2 $\pm 5\%$, $\frac{1}{3}$ W	R401865
R53	2k2 $\pm 5\%$, $\frac{1}{3}$ W	R401225
R54	100 $\pm 5\%$, $\frac{1}{3}$ W	R401104
R55	100 $\pm 5\%$, $\frac{1}{3}$ W	R401104
R56	1k0 $\pm 5\%$, $\frac{1}{3}$ W	R401105
R57	3k3 $\pm 5\%$, $\frac{1}{3}$ W	R401335
R58	10k $\pm 5\%$, $\frac{1}{3}$ W	R401106
R59	10k $\pm 5\%$, $\frac{1}{3}$ W	R401106
R60	15k $\pm 5\%$, $\frac{1}{3}$ W	R401156
R61	470 $\pm 5\%$, $\frac{1}{3}$ W	R401474
R62	22R $\pm 5\%$, $\frac{1}{3}$ W	R401223
R63	22k $\pm 5\%$, $\frac{1}{3}$ W	R401226
R64	680 $\pm 5\%$, $\frac{1}{3}$ W	R401684
R65	22k $\pm 5\%$, $\frac{1}{3}$ W	R401226
R66	47k $\pm 5\%$, $\frac{1}{3}$ W	R401476
R67	1k0 $\pm 5\%$, $\frac{1}{3}$ W	R401105
R68	470 $\pm 5\%$, $\frac{1}{3}$ W	R401474
R69	220 $\pm 5\%$, $\frac{1}{3}$ W	R401224

CIRCUIT REF.	DESCRIPTION	PART NO.
	RESISTORS (continued)	
R69	220 $\pm$ 5%, $\frac{1}{3}$ W	R401224
R70	220 $\pm$ 5%, $\frac{1}{3}$ W	R401224
R71	75R $\pm$ 1%, 0.4W	R432753
R72	10k $\pm$ 5%, $\frac{1}{3}$ W	R401106
R73	10k $\pm$ 5%, $\frac{1}{3}$ W	R401106
R74	10k $\pm$ 5%, $\frac{1}{3}$ W	R401106
R75	10k $\pm$ 5%, $\frac{1}{3}$ W	R401106
R76	4k7 $\pm$ 5%, $\frac{1}{3}$ W	R401475
R77	4k7 $\pm$ 5%, $\frac{1}{3}$ W	R401475
R78	Not fitted	—
R79	270 $\pm$ 5%, $\frac{1}{3}$ W	R401274
R80	10k $\pm$ 5%, $\frac{1}{3}$ W	R401106
R81	47k $\pm$ 5%, $\frac{1}{3}$ W	R401476
R82	47k $\pm$ 5%, $\frac{1}{3}$ W	R401476
R83	47k $\pm$ 5%, $\frac{1}{3}$ W	R401476
R84	10k $\pm$ 5%, $\frac{1}{3}$ W	R401106
R85	47k $\pm$ 5%, $\frac{1}{3}$ W	R401476
R86	5k6 $\pm$ 5%, $\frac{1}{3}$ W	R401565
R87	4k7 $\pm$ 5%, $\frac{1}{3}$ W	R401475
R88	2k2 $\pm$ 5%, $\frac{1}{3}$ W	R401225
R89	1k0 $\pm$ 5%, $\frac{1}{3}$ W	R401105
R90	10k $\pm$ 5%, $\frac{1}{3}$ W	R401106
R91	10k $\pm$ 5%, $\frac{1}{3}$ W	R401106
R92	470 $\pm$ 5%, $\frac{1}{3}$ W	R401474
R93	150 $\pm$ 5%, $\frac{1}{3}$ W	R401154
R94	10k $\pm$ 5%, $\frac{1}{3}$ W	R401106
R95	Not fitted	—
R96	10k $\pm$ 5%, $\frac{1}{3}$ W	R401106
R97	10k $\pm$ 5%, $\frac{1}{3}$ W	R401106
R98	100 $\pm$ 5%, $\frac{1}{3}$ W	R401104
R99	100 $\pm$ 5%, $\frac{1}{3}$ W	R401104
R100	100 $\pm$ 5%, $\frac{1}{3}$ W	R401104
R101	4k7 $\pm$ 5%, $\frac{1}{3}$ W	R401475
R102	10k $\pm$ 5%, $\frac{1}{3}$ W	R401106

CIRCUIT REF.	DESCRIPTION	PART NO.
	RESISTORS (continued)	
R103	100 $\pm$ 5%, $\frac{1}{3}$ W	R401104
R104	6k8 $\pm$ 5%, $\frac{1}{3}$ W	R401685
R105	1k0 $\pm$ 5%, $\frac{1}{3}$ W	R401105
R106	Not fitted	—
R107	560 $\pm$ 5%, $\frac{1}{3}$ W	R401564
R108	330 $\pm$ 5%, $\frac{1}{3}$ W	R401334
R109	1k0 $\pm$ 5%, $\frac{1}{3}$ W	R401105
R110	6k8 $\pm$ 5%, $\frac{1}{3}$ W	R401685
R111	100 $\pm$ 5%, $\frac{1}{3}$ W	R401104
R112	10k $\pm$ 5%, $\frac{1}{3}$ W	R401106
R113	10k $\pm$ 5%, $\frac{1}{3}$ W	R401106
R114	220 $\pm$ 5%, $\frac{1}{3}$ W	R401224
R115	100 $\pm$ 5%, $\frac{1}{3}$ W	R401104
R116	100 $\pm$ 5%, $\frac{1}{3}$ W	R401104
R117	10k $\pm$ 5%, $\frac{1}{3}$ W	R401106
R118	Not fitted	—
R119	4k7 $\pm$ 5%, $\frac{1}{3}$ W	R401475
R120	10k $\pm$ 5%, $\frac{1}{3}$ W	R401106
R121	100k $\pm$ 5%, $\frac{1}{3}$ W	R401107
R122	330k $\pm$ 5%, $\frac{1}{3}$ W	R401337
R123	180k $\pm$ 5%, $\frac{1}{3}$ W	R401187
R124	180k $\pm$ 5%, $\frac{1}{3}$ W	R401187
R125	68k $\pm$ 5%, $\frac{1}{3}$ W	R401686
R126	68k $\pm$ 5%, $\frac{1}{3}$ W	R401686
R127	470k $\pm$ 5%, $\frac{1}{3}$ W	R401477
R128	10k $\pm$ 5%, $\frac{1}{3}$ W	R401106
R129	10k $\pm$ 5%, $\frac{1}{3}$ W	R401106
R130	1k5 $\pm$ 5%, $\frac{1}{3}$ W	R401155
R131	22k $\pm$ 5%, $\frac{1}{3}$ W	R401226
R132	10k $\pm$ 5%, $\frac{1}{3}$ W	R401106
R133	15k $\pm$ 5%, $\frac{1}{3}$ W	R401156
R134	100k $\pm$ 5%, $\frac{1}{3}$ W	R401107
R135	100k $\pm$ 5%, $\frac{1}{3}$ W	R401107
R136	470 $\pm$ 5%, $\frac{1}{3}$ W	R401474

CIRCUIT REF.	DESCRIPTION	PART NO.
	RESISTORS (continued)	
R137	1M0 $\pm 10\%$, $\frac{1}{3}$ W	R401108
R138	Not fitted	—
R139	1k0 $\pm 5\%$, $\frac{1}{3}$ W	R401105
R140	1k0 $\pm 5\%$, $\frac{1}{3}$ W	R401105
R141	1k0 $\pm 5\%$, $\frac{1}{3}$ W	R401105
R142	1k0 $\pm 5\%$, $\frac{1}{3}$ W	R401105
R143	33R $\pm 5\%$, $\frac{1}{3}$ W	R401333
R144	680 $\pm 5\%$, $\frac{1}{3}$ W	R401684
R145	33R $\pm 5\%$, $\frac{1}{3}$ W	R401333
R146	270 $\pm 5\%$, $\frac{1}{3}$ W	R401274
R147	1k0 $\pm 5\%$, $\frac{1}{3}$ W	R401105
R148	100k $\pm 5\%$, $\frac{1}{3}$ W	R401107
R149	68k $\pm 5\%$, $\frac{1}{3}$ W	R401686
R150	1k0 $\pm 5\%$, $\frac{1}{3}$ W	R401105
R151	Not fitted	—
R152	4k7 $\pm 5\%$, $\frac{1}{3}$ W	R401475
R153	1k0 $\pm 5\%$, $\frac{1}{3}$ W	R401105
R154	1k8 $\pm 5\%$, $\frac{1}{3}$ W	R401185
R155	18k $\pm 5\%$, $\frac{1}{3}$ W	R401186
R156	470 $\pm 5\%$, $\frac{1}{3}$ W	R401474
R157	75R $\pm 1\%$, 0.4W	R432753
R158	680 $\pm 5\%$, $\frac{1}{3}$ W	R401684
R159	470 $\pm 5\%$, $\frac{1}{3}$ W	R401474
R160	4k7 $\pm 5\%$, $\frac{1}{3}$ W	R401475
R161	1k5 $\pm 5\%$, $\frac{1}{3}$ W	R401155
R162	680 $\pm 5\%$, $\frac{1}{3}$ W	R401684
R163	1k0 $\pm 5\%$, $\frac{1}{3}$ W	R401105
R164	4k7 $\pm 5\%$, $\frac{1}{3}$ W	R401475
R165	2k7 $\pm 5\%$, $\frac{1}{3}$ W	R401275
R166	75R $\pm 1\%$, 0.4W	R432753
R167	1M0 $\pm 10\%$, $\frac{1}{3}$ W	R401108
R168	2k7 $\pm 5\%$, $\frac{1}{3}$ W	R401275
R169	4k7 $\pm 5\%$, $\frac{1}{3}$ W	R401475
R170	27k $\pm 5\%$, $\frac{1}{3}$ W	R401276

CIRCUIT REF.	DESCRIPTION	PART NO.
	RESISTORS (continued)	
R171	2k7 $\pm 5\%$, $\frac{1}{3}$ W	R401275
R172	220 $\pm 5\%$, $\frac{1}{3}$ W	R401224
R173	100k $\pm 5\%$, $\frac{1}{3}$ W	R401107
R174	100 $\pm 5\%$, $\frac{1}{3}$ W	R401104
R175	1k0 $\pm 5\%$, $\frac{1}{3}$ W	R401105
R176	4k7 $\pm 5\%$, $\frac{1}{3}$ W	R401475
R177	680 $\pm 5\%$, $\frac{1}{3}$ W	R401684
R178	680 $\pm 5\%$, $\frac{1}{3}$ W	R401684
R179	15k $\pm 5\%$, $\frac{1}{3}$ W	R401156
R180	10k $\pm 5\%$, $\frac{1}{3}$ W	R401106
R181	22k $\pm 5\%$, $\frac{1}{3}$ W	R401226
R182	47k $\pm 5\%$, $\frac{1}{3}$ W	R401476
R183	100k $\pm 5\%$, $\frac{1}{3}$ W	R401107
R184	10k $\pm 5\%$, $\frac{1}{3}$ W	R401106
R185	220 $\pm 5\%$, $\frac{1}{3}$ W	R401224
R186	220 $\pm 5\%$, $\frac{1}{3}$ W	R401224
R187	39k $\pm 5\%$, $\frac{1}{3}$ W	R401396
R188	1k0 $\pm 5\%$, $\frac{1}{3}$ W	R401105
R189	1k0 $\pm 5\%$, $\frac{1}{3}$ W	R401105
R190	3k9 $\pm 5\%$, $\frac{1}{3}$ W	R401395
R191	10k $\pm 5\%$, $\frac{1}{3}$ W	R401106
R192	100k $\pm 5\%$, $\frac{1}{3}$ W	R401107
R193	47k $\pm 5\%$, $\frac{1}{3}$ W	R401476
R194	6k8 $\pm 5\%$, $\frac{1}{3}$ W	R401685
R195	82k $\pm 5\%$, $\frac{1}{3}$ W	R401826
R196	10k $\pm 5\%$, $\frac{1}{3}$ W	R401106
R197	12k $\pm 5\%$, $\frac{1}{3}$ W	R401126
R198	15k $\pm 5\%$, $\frac{1}{3}$ W	R401156
R199	3k3 $\pm 5\%$, $\frac{1}{3}$ W	R401335
R200	10k $\pm 5\%$, $\frac{1}{3}$ W	R401106
R201	10k $\pm 5\%$, $\frac{1}{3}$ W	R401106
R202	4k7 $\pm 5\%$, $\frac{1}{3}$ W	R401475
R203	47k $\pm 5\%$, $\frac{1}{3}$ W	R401476
R204	10k $\pm 5\%$, $\frac{1}{3}$ W	R401106

CIRCUIT REF.	DESCRIPTION	PART NO.
	RESISTORS (continued)	
R205	4k7 $\pm 5\%$, $\frac{1}{3}W$	R401475
R206	47k $\pm 5\%$, $\frac{1}{3}W$	R401476
R207	Not fitted	—
R208	47k $\pm 5\%$, $\frac{1}{3}W$	R401476
R209	100k $\pm 5\%$, $\frac{1}{3}W$	R401107
R210	47k $\pm 5\%$, $\frac{1}{3}W$	R401476
R211	100k $\pm 5\%$, $\frac{1}{3}W$	R401107
R212	100k $\pm 5\%$, $\frac{1}{3}W$	R401107
R213	100k $\pm 5\%$, $\frac{1}{3}W$	R401107
R214	47k $\pm 5\%$, $\frac{1}{3}W$	R401476
R215	4k7 $\pm 5\%$, $\frac{1}{3}W$	R401475
R216	4k7 $\pm 5\%$, $\frac{1}{3}W$	R401475
R217	150k $\pm 5\%$, $\frac{1}{3}W$	R401157
R218	6k8 $\pm 5\%$, $\frac{1}{3}W$	R401685
R219	470 $\pm 5\%$, $\frac{1}{3}W$	R401474
R220	75R $\pm 1\%$, 0.4W	R432753
R221	4M7 $\pm 10\%$, $\frac{1}{3}W$	R401478
R222	8k2 $\pm 5\%$, $\frac{1}{3}W$	R401825
R223	330 $\pm 5\%$, $\frac{1}{3}W$	R401334
R224	470 $\pm 5\%$, $\frac{1}{3}W$	R401474
R225	100 $\pm 5\%$, $\frac{1}{3}W$	R401104
R226	100 $\pm 5\%$, $\frac{1}{3}W$	R401104
R227	Not fitted	—
R228	100 $\pm 5\%$, $\frac{1}{3}W$	R401104
R229	10k $\pm 5\%$, $\frac{1}{3}W$	R401106
R230	22k $\pm 5\%$, $\frac{1}{3}W$	R401226
R231	22k $\pm 5\%$, $\frac{1}{3}W$	R401226
R232	5k6 $\pm 5\%$, $\frac{1}{3}W$	R401565
R233	2k2 $\pm 5\%$, $\frac{1}{3}W$	R401225
R234	3k3 $\pm 5\%$, $\frac{1}{3}W$	R401335
R235	150k $\pm 5\%$, $\frac{1}{3}W$	R401157
R236	22k $\pm 5\%$, $\frac{1}{3}W$	R401226
R237	15k $\pm 5\%$, $\frac{1}{3}W$	R401156
R238	100 $\pm 5\%$, $\frac{1}{3}W$	R401104

CIRCUIT REF.	DESCRIPTION	PART NO.
	RESISTORS (continued)	
R239	10k $\pm 5\%$, $\frac{1}{3}$ W	R401106
R240	10k $\pm 5\%$, $\frac{1}{3}$ W	R401106
R241	6k8 $\pm 5\%$, $\frac{1}{3}$ W	R401685
R242	47k $\pm 5\%$, $\frac{1}{3}$ W	R401476
R243	100k $\pm 5\%$, $\frac{1}{3}$ W	R401107
R244	68k $\pm 5\%$, $\frac{1}{3}$ W	R401686
R245	100 $\pm 5\%$, $\frac{1}{3}$ W	R401104
R246 – R253	22k $\pm 5\%$, $\frac{1}{3}$ W	R401226
R254	470k $\pm 5\%$, $\frac{1}{3}$ W	R401477
R255	47k $\pm 5\%$, $\frac{1}{3}$ W	R401476
R256	100k $\pm 5\%$, $\frac{1}{3}$ W	R401107
R257	Not fitted	—
R258	4k7 $\pm 5\%$, $\frac{1}{3}$ W	R401475
R259	680 $\pm 5\%$, $\frac{1}{3}$ W	R401684
R260	470 $\pm 5\%$, $\frac{1}{3}$ W	R401474
R261	4k7 $\pm 5\%$, $\frac{1}{3}$ W	R401475
R262	680 $\pm 5\%$, $\frac{1}{3}$ W	R401684
R263	470 $\pm 5\%$, $\frac{1}{3}$ W	R401474
R264	4k7 $\pm 5\%$, $\frac{1}{3}$ W	R401475
R265	680 $\pm 5\%$, $\frac{1}{3}$ W	R401684
R266	470 $\pm 5\%$, $\frac{1}{3}$ W	R401474
R267	4k7 $\pm 5\%$, $\frac{1}{3}$ W	R401475
R268	680 $\pm 5\%$, $\frac{1}{3}$ W	R401684
R269	470 $\pm 5\%$, $\frac{1}{3}$ W	R401474
R270	4k7 $\pm 5\%$, $\frac{1}{3}$ W	R401475
R271	680 $\pm 5\%$, $\frac{1}{3}$ W	R401684
R272	470 $\pm 5\%$, $\frac{1}{3}$ W	R401474
R273	4k7 $\pm 5\%$, $\frac{1}{3}$ W	R401475
R274	1k2 $\pm 5\%$, $\frac{1}{3}$ W	R401125
R275	470 $\pm 5\%$, $\frac{1}{3}$ W	R401474
R276 – R281	680 $\pm 5\%$, $\frac{1}{3}$ W	R401684
R282 – R287	1k5 $\pm 5\%$, $\frac{1}{3}$ W	R401155
R288 – R294	4k7 $\pm 5\%$, $\frac{1}{3}$ W	R401475
R295	1k0 $\pm 5\%$, $\frac{1}{3}$ W	R401105

CIRCUIT REF.	DESCRIPTION	PART NO.
	RESISTORS (continued)	
R296	75R $\pm 1\%$, 0.4W	R432753
R297	4k7 $\pm 5\%$, $\frac{1}{3}$ W	R401475
R298	1k0 $\pm 5\%$, $\frac{1}{3}$ W	R401105
R299	75R $\pm 1\%$, $\frac{1}{3}$ W	R432753
R300	4k7 $\pm 5\%$, $\frac{1}{3}$ W	R401475
R301	1k0 $\pm 5\%$, $\frac{1}{3}$ W	R401105
R302	75R $\pm 1\%$, 0.4W	R432753
R303	4k7 $\pm 5\%$, $\frac{1}{3}$ W	R401475
R304	1k0 $\pm 5\%$, $\frac{1}{3}$ W	R401105
R305	75R $\pm 1\%$, 0.4W	R432753
R306	4k7 $\pm 5\%$, $\frac{1}{3}$ W	R401475
R307	1k0 $\pm 5\%$, $\frac{1}{3}$ W	R401105
R308	75R $\pm 1\%$, 0.4W	R432753
R309	4k7 $\pm 5\%$, $\frac{1}{3}$ W	R401475
R310	1k0 $\pm 5\%$, $\frac{1}{3}$ W	R401105
R311	75R $\pm 1\%$, 0.4W	R432753
R312	1k0 $\pm 5\%$, $\frac{1}{3}$ W	R401105
R313	330 $\pm 5\%$, $\frac{1}{3}$ W	R401334
R314	220k $\pm 5\%$, $\frac{1}{3}$ W	R401227
R315	100k $\pm 5\%$, $\frac{1}{3}$ W	R401107
R316	470 $\pm 5\%$, $\frac{1}{3}$ W	R401474
RV1	10k, variable	R492106
RV2	470, variable	R492474
RV3	4k7, variable	R492475
RV4	47k, variable	R492476
RV5	470, variable	R492474
RV6	47k, variable	R492476
RV7	47k, variable	R492476
RV8	100k, variable	R492107
	CONNECTORS	
SK1	Socket, 16-pin DIL	R808016
SK2	Socket, 16-pin DIL	R808016
SK3	2-part connector, 16-pin	R810016
SK4	2-part connector, 10-pin	R810010

CIRCUIT REF.	DESCRIPTION	PART NO.
	CONNECTORS (continued)	
SK5	2-part connector, 16-pin	R810116
SK6	2-part connector, 16-pin	R810116
SK7	2-part connector, 3-pin	R810003
SK8	Socket, 16-pin DIL	R808016
SK9	2-part connector, 5-pin	R810005
SK10	2-part connector, 3-pin	R810003
	TRANSFORMERS	
T1	Type B	R650201
T2	Type A	R650100
T3	Type C	R650302
	TRANSISTORS	
TR1	ZTX212AL	R348212
TR2	ZTX107L	R348107
TR3	E421	R325421
TR4	ZTX212AL	R348212
TR5	ZTX107L	R348107
TR6	ZTX107L	R348107
TR7	ZTX107L	R348107
TR8	BFR81	R322081
TR9 – TR16	ZTX107	R348107
TR17	BRF81	R322081
TR18	ZTX212AL	R348212
TR19	ZTX107L	R348107
TR20	ZTX212AL	R348212
TR21	Not fitted	—
TR22	2N2369A	R312369
TR23	ZTX212AL	R348212
TR24	E176	R325176
TR25	E300	R325300
TR26	E176	R325176
TR27	2N2369A	R312369
TR28	2N2369A	R312369
TR29 – TR35	ZTX212	R348212
TR36	ZTX107L	R348107

CIRCUIT REF.	DESCRIPTION	PART NO.
	TRANSISTORS (continued)	
TR37	ZTX212AL	R348212
TR38	ZTX212AL	R348212
TR39	ZTX107L	R348107
TR40	ZTX107	R348107
TR41	ZTX212	R348212
TR42	ZTX107	R348107
TR43	ZTX212	R348212
TR44	MPS6521	R334653
TR45	ZTX107	R348107
TR46	2N2369A	R312369
TR47	ZTX212AL	R348212
TR48	ZTX107	R348107
TR49	ZTX212	R348212
TR50	ZTX107	R348107
TR51	ZTX107	R348107
TR52	ZTX212	R348212
TR53	ZTX107	R348107
TR54	E210	R325210
TR55	ZTX212	R348212
TR56	E176	R325176
TR57	78L12	R330783
TR58	E300	R325300
TR60	ZTX212	R348212
TR61	ZTX212	R348212
TR62	ZTX107	R348107
TR63	ZTX107	R348107
TR64	ZTX212	R348212
TR65	ZTX212	R348212
TR66	ZTX212	R348212
TR67	ZTX107	R348107
TR68	ZTX107	R348107
TR69	ZTX212	R348212
TR70	ZTX212	R348212
TR71	ZTX212	R348212

CIRCUIT REF.	DESCRIPTION	PART NO.
	TRANSISTORS (continued)	
TR72	ZTX107	R348107
TR73	ZTX107	R348107
TR74	ZTX212	R348212
TR76	ZTX212	R348212
TR77	ZTX107	R348107
TR78	ZTX107	R348107
TR79	ZTX212	R348212
TR80	ZTX212	R348212
TR81	ZTX212	R348212
TR82	ZTX107	R348107
TR83	ZTX107	R348107
TR84	ZTX212	R348212
TR85	ZTX212	R348212
TR86	ZTX212	R348212
TR87	ZTX107	R348107
TR88	ZTX107	R348107
TR89	ZTX212	R348212

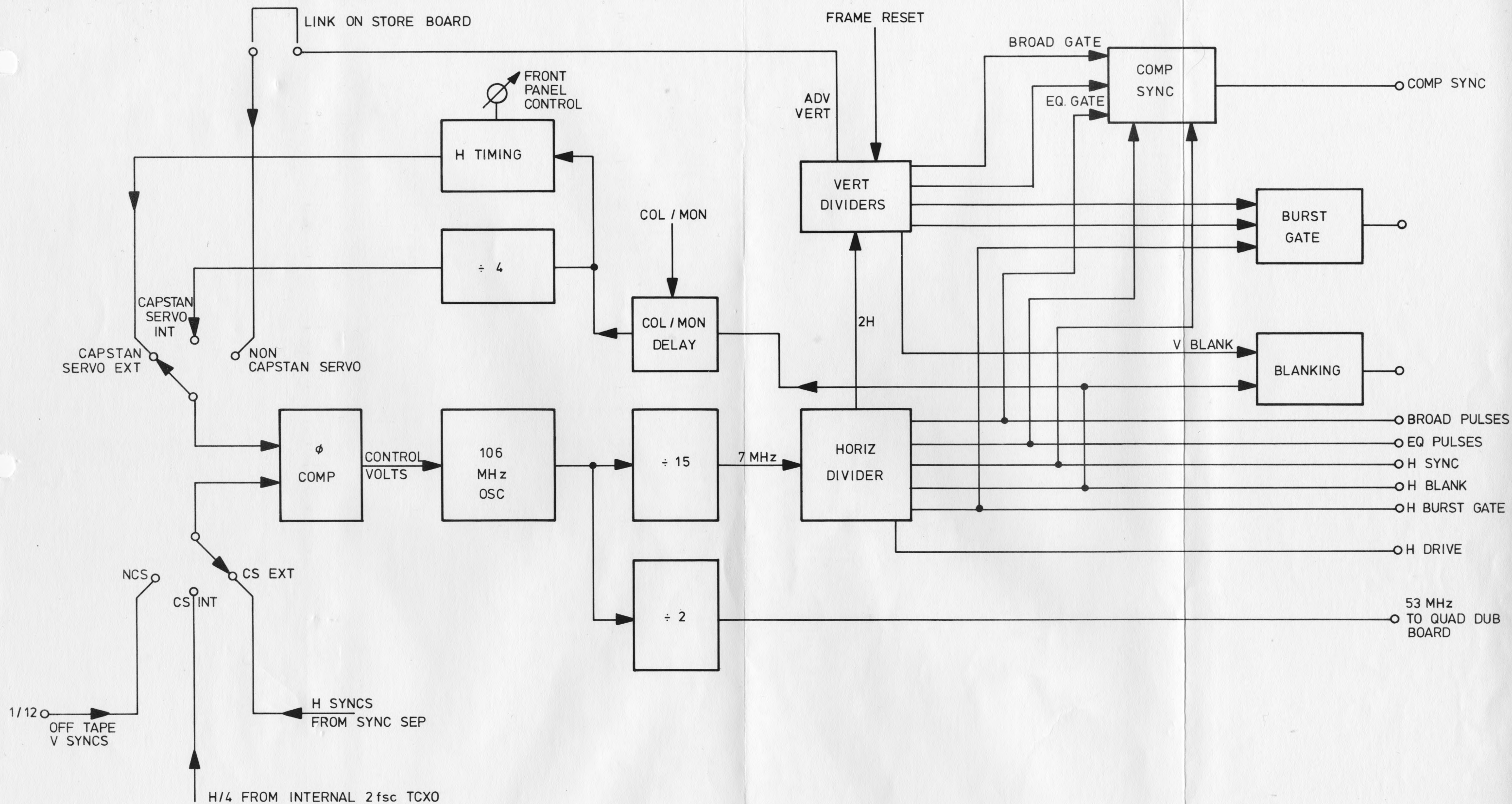


FIGURE 1 BLOCK DIAGRAM MASTER OSCILLATOR WITH HORIZONTAL AND VERTICAL DIVIDERS

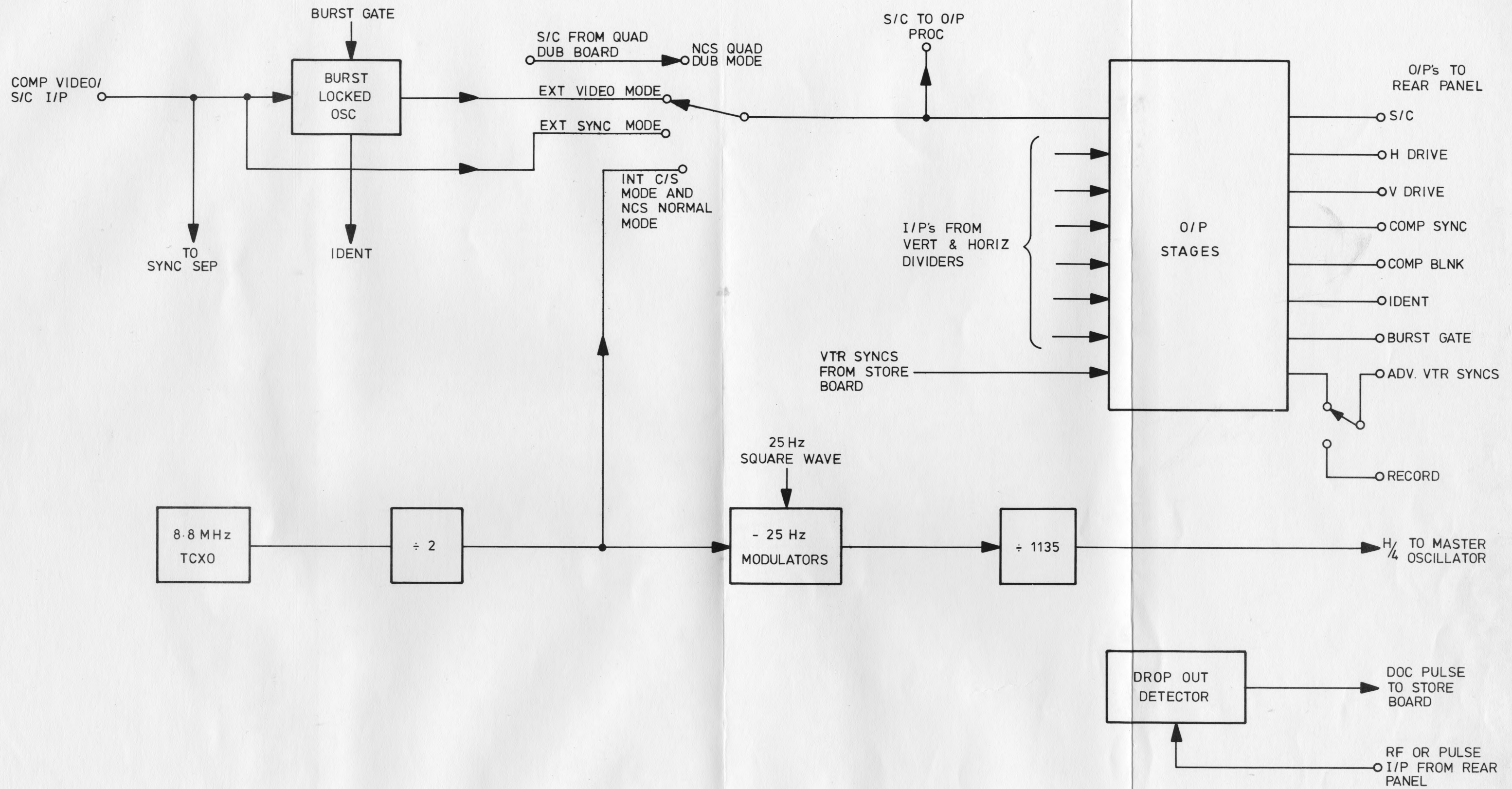


FIGURE 2 BLOCK DIAGRAM, LOCKING INPUT INTERFACES AND OUTPUT STAGES

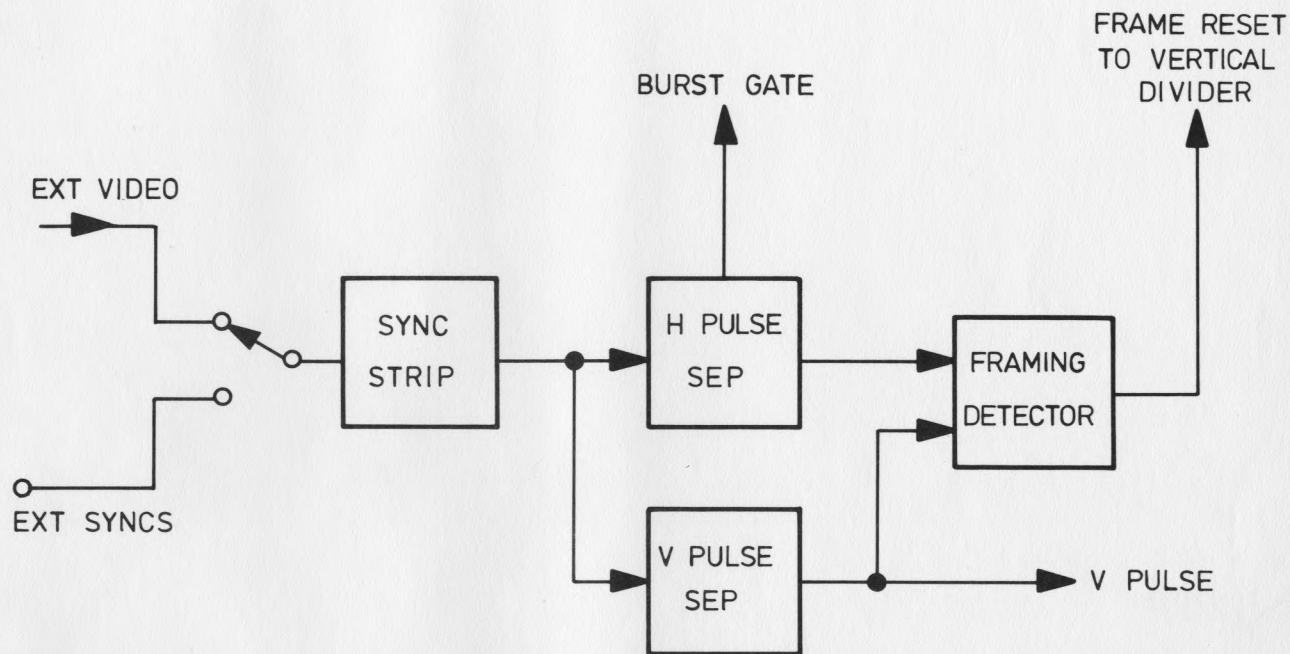


FIGURE 3 BLOCK DIAGRAM, ADVANCED VTR LOCK CONTROL

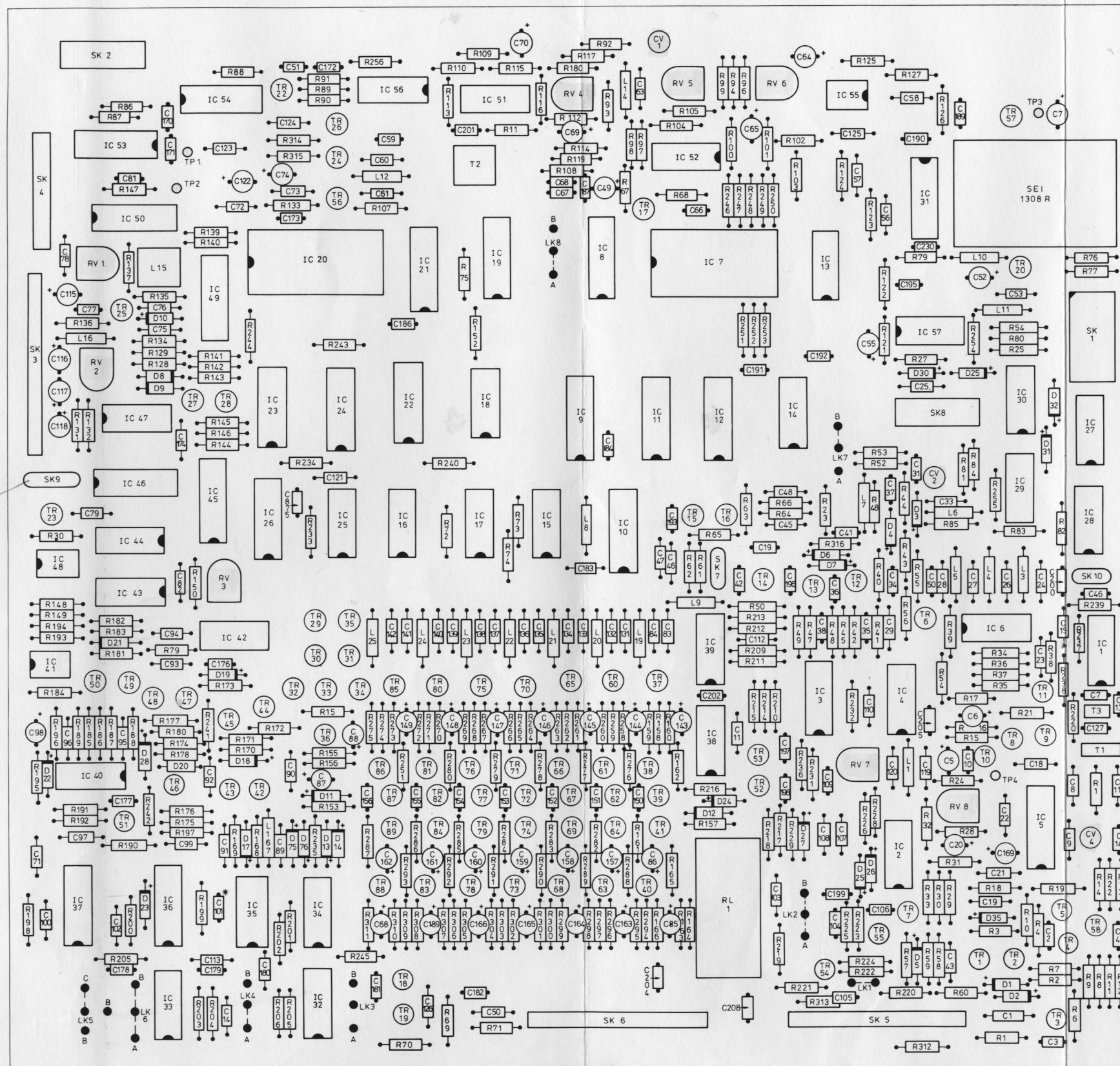
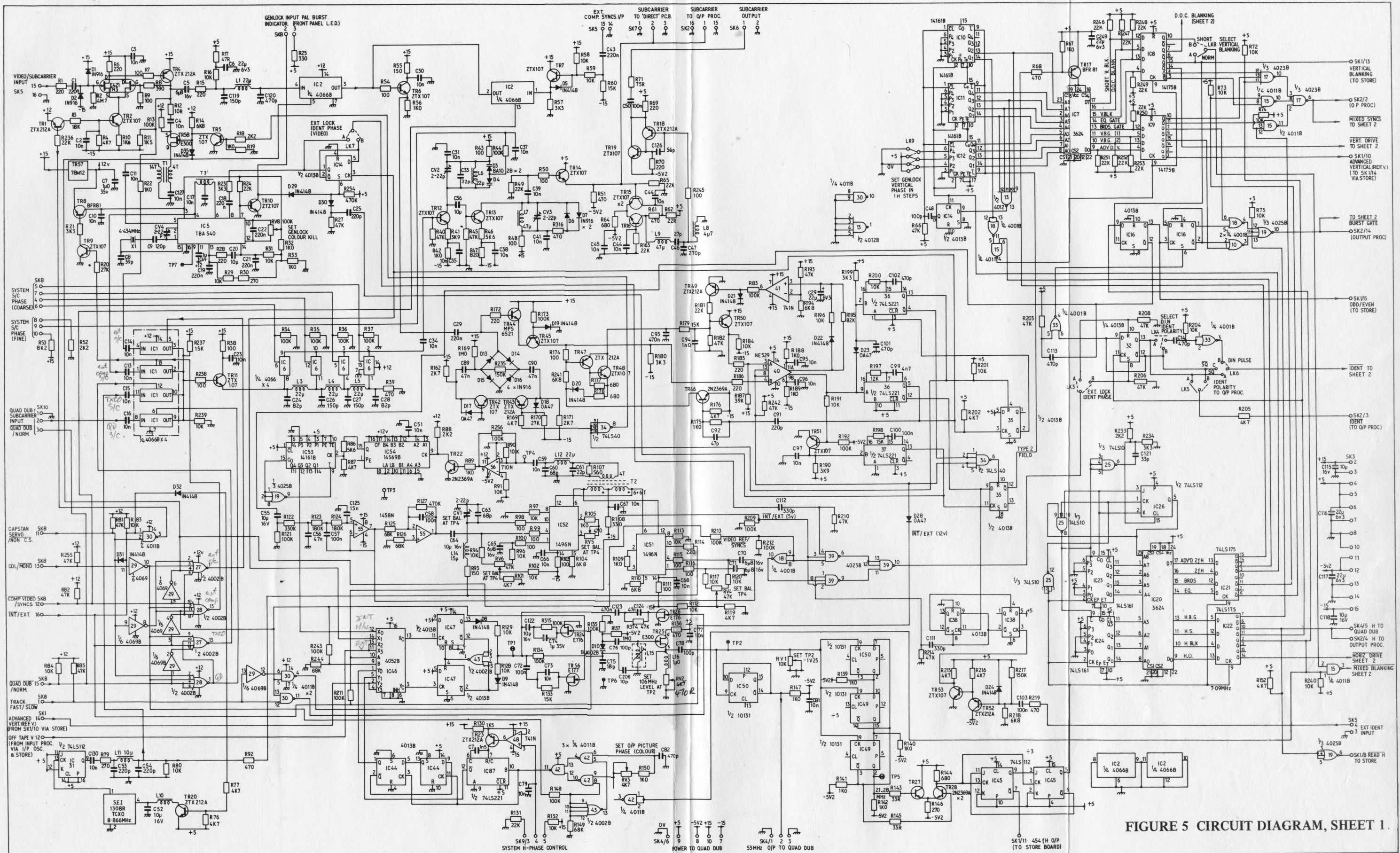
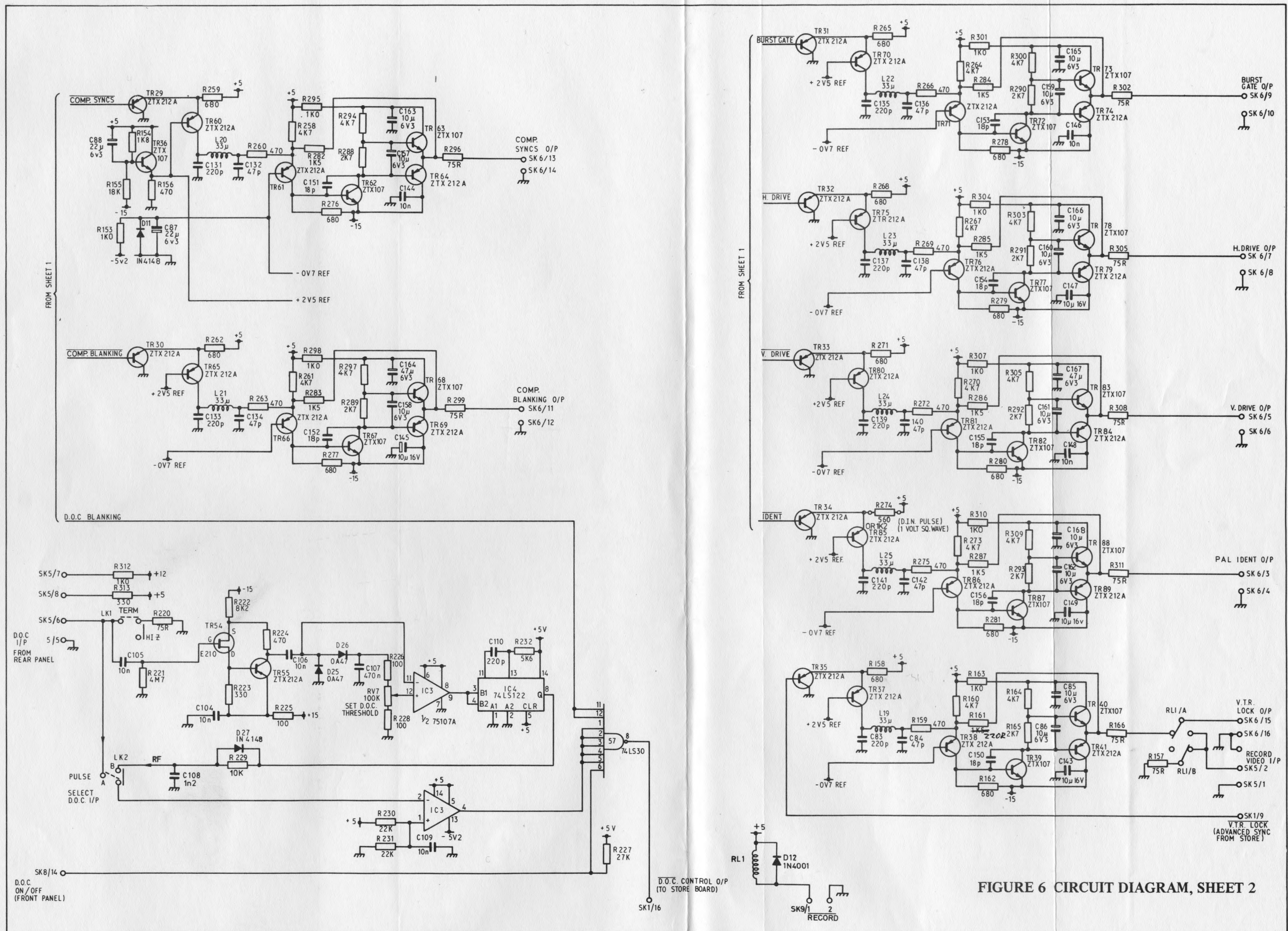


FIGURE 4 COMPONENT LAYOUT





QUAD DUB
IVC PCB GL211

INTRODUCTION	1
CIRCUIT DESCRIPTION	1
ADJUSTMENTS	1
CONNECTIONS	1
TEST POINTS	2
COMPONENT SCHEDULE	3

FIGURE 1	BLOCK DIAGRAM
FIGURE 2	COMPONENT LAYOUT
FIGURE 3	CIRCUIT DIAGRAM

QUAD DUB

IVC PCB GL211

INTRODUCTION

The circuitry on the Quad Dub card can only be selected when the TBC-2002 is in the NON CAPSTAN SERVO mode.

The purpose of the card is to produce a PAL subcarrier signal (fSC) which is correctly related in frequency to the outgoing horizontal (fH) and vertical (fV) scanning frequencies. The correct relationship for PAL is:—

$$f_{SC} = \frac{1135f_H}{4} + \frac{f_V}{2}$$

CIRCUIT DESCRIPTION

The Quad Dub card receives 53MHz ECL clock pulses from the Sync Pulse Generator card via SK1/2. These clock pulses are input to a divide-by-4 circuit, IC4, which drives an ECL to TTL converter comprising TR1 and TR2. The TTL level signal at the collector of TR2 clocks a “ring of 3” circuit (IC8 and IC3/5). The outputs of this “ring of 3” circuit are applied to IC9 which ensures that the circuit always runs with a 001 sequence at the Q outputs. Hence, the 3 phase Q outputs enable each of the tri-state outputs of PROMs IC5, IC6, IC7 in turn.

The 9-bit address word to the PROMs is derived from a 10-bit binary counter, IC1, using bits 2 – 10 only. The counter is clocked, via IC2/1, on the positive-going edge of the horizontal frequency pulse, fH, input via SK1/5 from the Sync Pulse Generator card. When a count of 624 is reached, IC2/13 goes low. On the next fH pulse IC3/8 goes high and resets IC1/11 via C1.

Each PROM outputs an 8-bit TTL level data word. The output enabled by the “ring of 3” circuit is fed via level shifting resistors to ECL latches IC10 and IC11. These latches are clocked by a 13.3MHz pulsetrain from the divide-by-4 circuit IC4, and their outputs are applied to an

8-bit digital-to-analogue converter IC12. The current output from IC12/15 feeds common-base amplifier TR3 whose collector is connected to a 4.43MHz bandpass filter L2, L3, C8, C9. The PAL subcarrier frequency sinewave at the output of this filter is buffered by emitter follower TR4 and is output from the card at pin B via a length of coaxial cable and plug PL3.

When the Quad Dub option is not selected, the QUAD DUB signal on pin A is high and presets IC4/12 so that the counter is inhibited. This QUAD DUB signal is derived from the switch on the front panel and is input via the Sync Pulse Generator card and PL3/3.

Links LK1, LK2 and LK3 enable the PROMs to be tested individually. These links are normally connected to their centre lug. A PROM is enabled when its associated link is connected to the lug marked 0, and inhibited when it is connected to the lug marked 5.

ADJUSTMENTS

LK1 — Normally in the centre position. For testing purposes it is linked to lug 5 to inhibit IC7, and to lug 0 to enable IC7.

LK2 — Normally in the centre position. For testing purposes it is linked to lug 5 to inhibit IC6, and to lug 0 to enable IC6.

LK3 — Normally in the centre position. For testing purposes it is linked to lug 5 to inhibit IC5, and to lug 0 to enable IC5.

CONNECTIONS

SK1	Input signals
1	Ground
2	53MHz input

CONNECTIONS (continued)

3	Ground
5	fH input
7	-15V
8	-5.2V
9	+5V
10	+15V

Pin A	PL3/3 QUAD DUB select
Pin B	PL3/1 Ground, (fSC)
	PL3/2 Quad Dub subcarrier fSC

TEST POINTS

TP1	53MHz input
TP2	fH input
TP3	PAL fSC output
TPE	Earth

This circuit is designed to provide a PAL subcarrier signal (fSC) which is related in frequency to the outgoing horizontal (fH) and vertical (fV) scanning frequencies. The correct relationship for PAL is:

$$f_{SC} = \frac{f_{H}}{2} + \frac{f_{V}}{2}$$

The Quad Dub card receives 53MHz fH clock pulses from the Sync Filter Generator card via SK1/2. These clock pulses are input to a divide-by-4 circuit, IC4, which drives an ECL to TTL converter comprising TR1 and TR2. The TTL-level signal at the collector of TR2 clocks a "ring of 3" circuit (IC3 and IC3/2). The output of this "ring of 3" circuit is applied to IC2, which generates the fSC signal. The fSC signal is always 0.01% accurate at the output. Hence, the fSC signal is applied to each of the fSC outputs of IC2, IC3, IC4, IC5, IC6, IC7, and IC8.

The 9-bit address word to the PAL is derived from a 10-bit binary counter, IC1, outputs 3 - 10 only. The counter is clocked via IC1/1, on the positive-going edge of the horizontal frequency pulse, fH, input via SK1/5 from the Sync Filter Generator card. When a count of 024 is reached, IC1/3 goes low. On the next fH pulse IC1/3 goes high and resets IC1/1 to 01.

Each fSC output is 8-bit TTL level data word. The output enabled by the "ring of 3" circuit is fed via level shifting resistors to BCL latch IC10 and IC11. These latches are clocked by a 13.3MHz pulse train from the divide-by-4 circuit, IC4, and their outputs are applied to an

INTRODUCTION

The circuitry on the Quad Dub card can only be selected when the TBC-2002 is in the NOM CAPTAIN SERVO mode.

The purpose of the card is to produce a PAL subcarrier signal (fSC) which is correctly related in frequency to the outgoing horizontal (fH) and vertical (fV) scanning frequencies. The correct relationship for PAL is:

$$f_{SC} = \frac{f_{H}}{2} + \frac{f_{V}}{2}$$

CIRCUIT DESCRIPTION

The Quad Dub card receives 53MHz fH clock pulses from the Sync Filter Generator card via SK1/2. These clock pulses are input to a divide-by-4 circuit, IC4, which drives an ECL to TTL converter comprising TR1 and TR2. The TTL-level signal at the collector of TR2 clocks a "ring of 3" circuit (IC3 and IC3/2). The output of this "ring of 3" circuit is applied to IC2, which generates the fSC signal. The fSC signal is always 0.01% accurate at the output. Hence, the fSC signal is applied to each of the fSC outputs of IC2, IC3, IC4, IC5, IC6, IC7, and IC8.

The 9-bit address word to the PAL is derived from a 10-bit binary counter, IC1, outputs 3 - 10 only. The counter is clocked via IC1/1, on the positive-going edge of the horizontal frequency pulse, fH, input via SK1/5 from the Sync Filter Generator card. When a count of 024 is reached, IC1/3 goes low. On the next fH pulse IC1/3 goes high and resets IC1/1 to 01.

Each fSC output is 8-bit TTL level data word. The output enabled by the "ring of 3" circuit is fed via level shifting resistors to BCL latch IC10 and IC11. These latches are clocked by a 13.3MHz pulse train from the divide-by-4 circuit, IC4, and their outputs are applied to an

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CIRCUIT REF.	DESCRIPTION	PART NO.
CAPACITORS		
C1	100pF, 63V	R511015
C2	100pF, 63V	R511015
C3	10nF, 25V	R501033
C4	100nF, 25V	R501043
C5	47 μ F, 6.3V	R544761
C6	100nF, 25V	R501043
C7	10nF, 25V	R501033
C8	27 μ F, 63V	R512765
C9	270 μ F, 63V	R512775
C10	10nF, 25V	R501033
C11	10nF, 25V	R501033
C12	10 μ F, 16V	R541062
C13	22 μ F, 6.3V	R542261
C14	22 μ F, 6.3V	R542261
C15	10 μ F, 16V	R541062
C16 – C24	10nF, 25V	R501033
C25	22 μ F, 6.3V	R542261
C26	10nF, 25V	R501033
INTEGRATED CIRCUITS		
IC1	4040B	R261040
IC2	4012B	R261012
IC3	74LS74	R240074
IC4	10131	R250131
IC5	74S473	R230473
IC6	74S473	R230473
IC7	74S473	R230473
IC8	74LS74	R240074
IC9	74LS27	R240027
IC10	10176	R250176
IC11	10131	R250131
IC12	10318	R250318
INDUCTORS		
L1	47 μ H	R620473
L2	47 μ H	R620473

CIRCUIT REF.	DESCRIPTION	PART NO.
	INDUCTORS (continued)	
L3	4.7 μ H	R620472
	RESISTORS	
R1	47k $\pm$ 5%, $\frac{1}{3}$ W	R401476
R2	47k $\pm$ 5%, $\frac{1}{3}$ W	R401476
R3	4k7 $\pm$ 5%, $\frac{1}{3}$ W	R401475
R4	Not fitted	—
R5	Not fitted	—
R6	47k $\pm$ 5%, $\frac{1}{3}$ W	R401476
R7	Not fitted	—
R8	1k0 $\pm$ 5%, $\frac{1}{3}$ W	R401105
R9	1k0 $\pm$ 5%, $\frac{1}{3}$ W	R401105
R10	1k0 $\pm$ 5%, $\frac{1}{3}$ W	R401105
R11	33R $\pm$ 5%, $\frac{1}{3}$ W	R401333
R12	330 $\pm$ 5%, $\frac{1}{3}$ W	R401334
R13	820 $\pm$ 5%, $\frac{1}{3}$ W	R401824
R14	33R $\pm$ 5%, $\frac{1}{3}$ W	R401333
R15	2k2 $\pm$ 5%, $\frac{1}{3}$ W	R401225
R16	2k2 $\pm$ 5%, $\frac{1}{3}$ W	R401225
R17	2k2 $\pm$ 5%, $\frac{1}{3}$ W	R401225
R18	2k2 $\pm$ 5%, $\frac{1}{3}$ W	R401225
R19	2k7 $\pm$ 5%, $\frac{1}{3}$ W	R401275
R20	2k7 $\pm$ 5%, $\frac{1}{3}$ W	R401275
R21	2k2 $\pm$ 5%, $\frac{1}{3}$ W	R401225
R22	2k2 $\pm$ 5%, $\frac{1}{3}$ W	R401225
R23	2k2 $\pm$ 5%, $\frac{1}{3}$ W	R401225
R24	2k2 $\pm$ 5%, $\frac{1}{3}$ W	R401225
R25	2k7 $\pm$ 5%, $\frac{1}{3}$ W	R401275
R26	2k7 $\pm$ 5%, $\frac{1}{3}$ W	R401275
R27	2k7 $\pm$ 5%, $\frac{1}{3}$ W	R401275
R28	2k7 $\pm$ 5%, $\frac{1}{3}$ W	R401275
R29	2k7 $\pm$ 5%, $\frac{1}{3}$ W	R401275
R30	2k7 $\pm$ 5%, $\frac{1}{3}$ W	R401275
R31	1k0 $\pm$ 5%, $\frac{1}{3}$ W	R401105
R32	1k0 $\pm$ 5%, $\frac{1}{3}$ W	R401105

CIRCUIT REF.	DESCRIPTION	PART NO.
	RESISTORS (continued)	
R33	1k0 $\pm 5\%$, $\frac{1}{3}$ W	R401105
R34	1k0 $\pm 5\%$, $\frac{1}{3}$ W	R401105
R35	1k0 $\pm 5\%$, $\frac{1}{3}$ W	R401105
R36	1k0 $\pm 5\%$, $\frac{1}{3}$ W	R401105
R37	1k0 $\pm 5\%$, $\frac{1}{3}$ W	R401105
R38	1k0 $\pm 5\%$, $\frac{1}{3}$ W	R401105
R39	27k $\pm 5\%$, $\frac{1}{3}$ W	R401276
R40	27k $\pm 5\%$, $\frac{1}{3}$ W	R401276
R41	470 $\pm 5\%$, $\frac{1}{3}$ W	R401474
R42	100 $\pm 5\%$, $\frac{1}{3}$ W	R401104
R43	1k8 $\pm 5\%$, $\frac{1}{3}$ W	R401185
R44	68R $\pm 5\%$, $\frac{1}{3}$ W	R401683
R45	Not fitted	—
	CONNECTOR	
SK1	2-part connector, 10-pin	R810110
	TRANSISTORS	
TR1	2N2369	R302369
TR2	2N2369	R302369
TR3	ZTX107L	R348107
TR4	ZTX107L	R348107

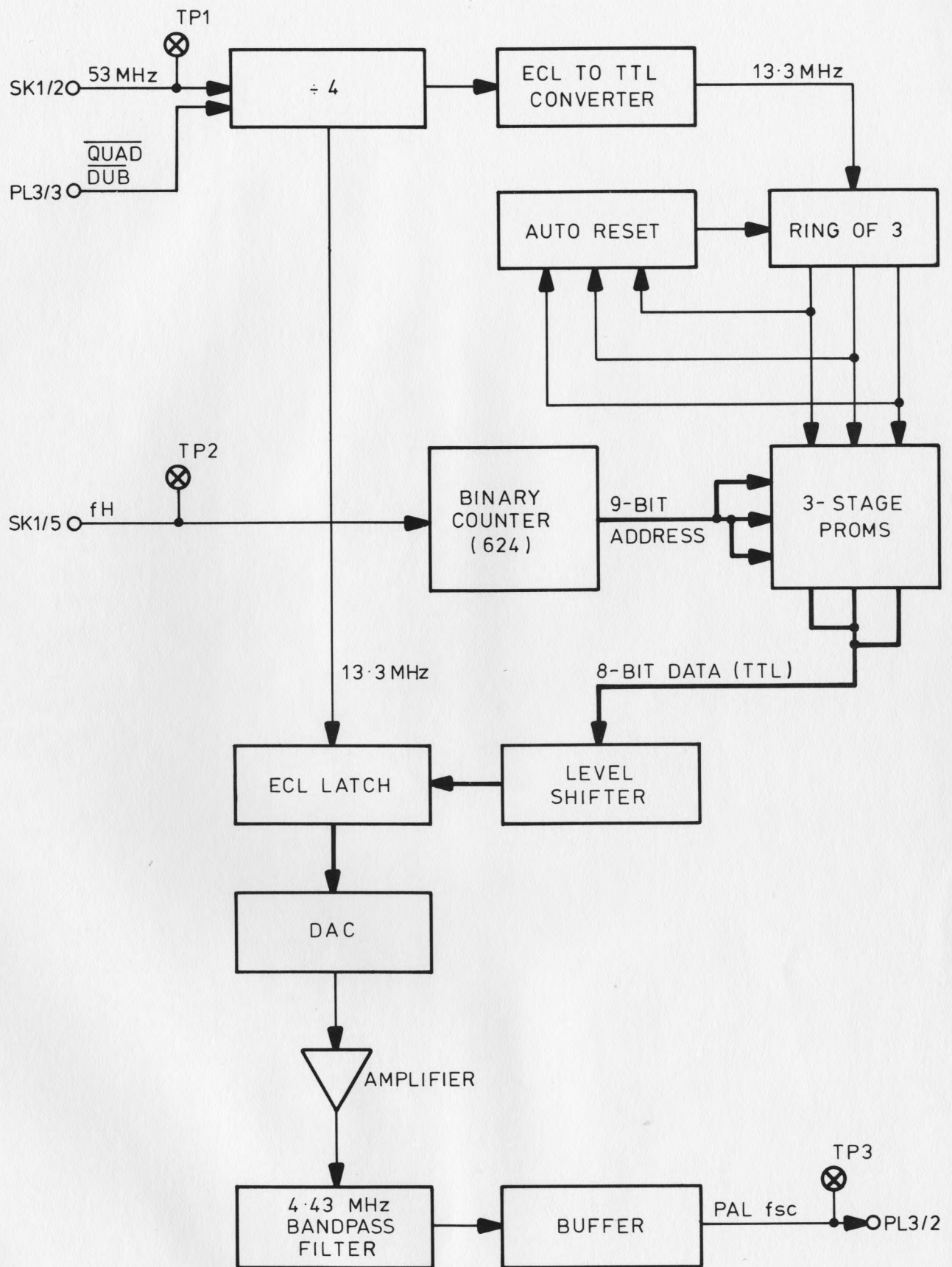


FIGURE 1 BLOCK DIAGRAM

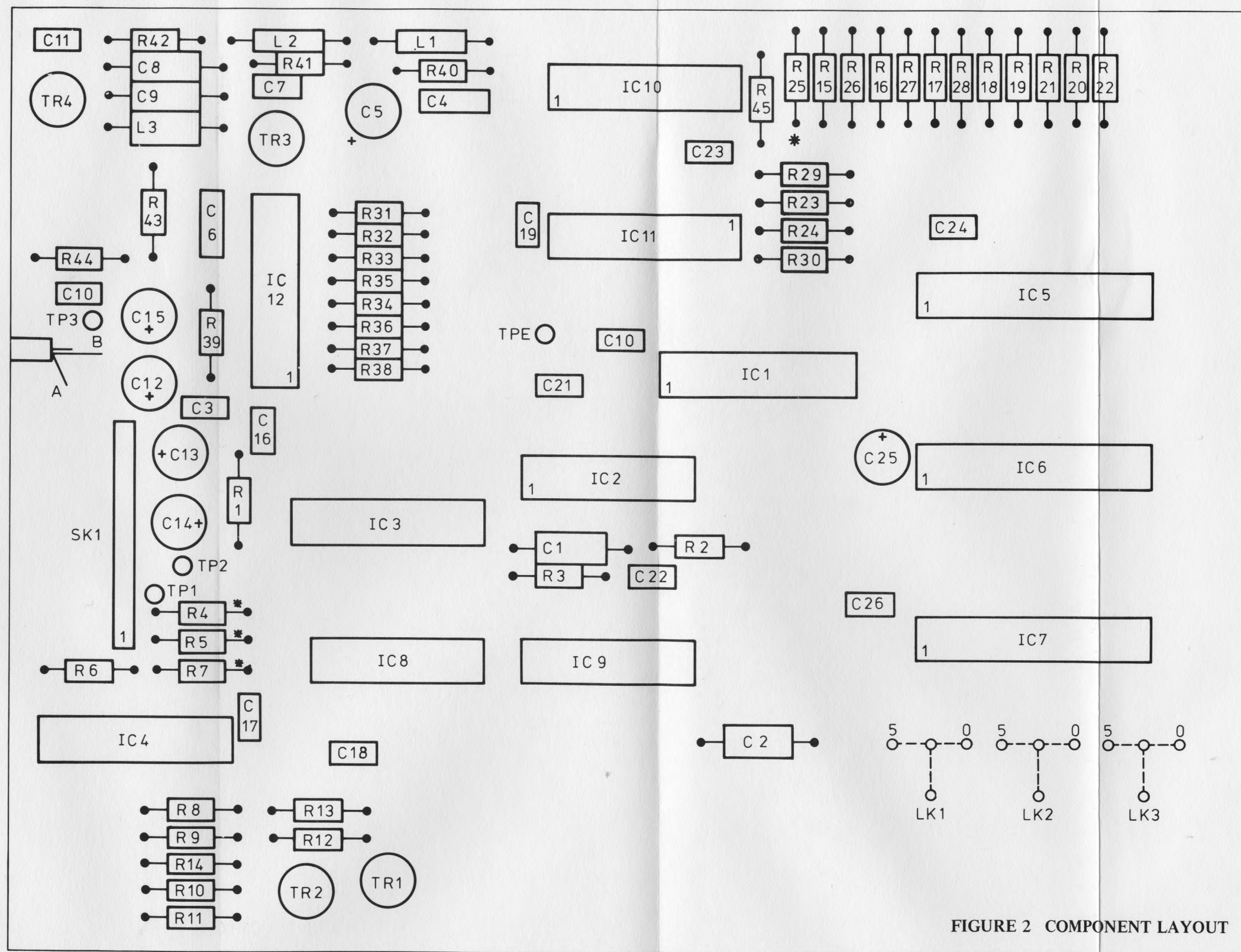


FIGURE 2 COMPONENT LAYOUT

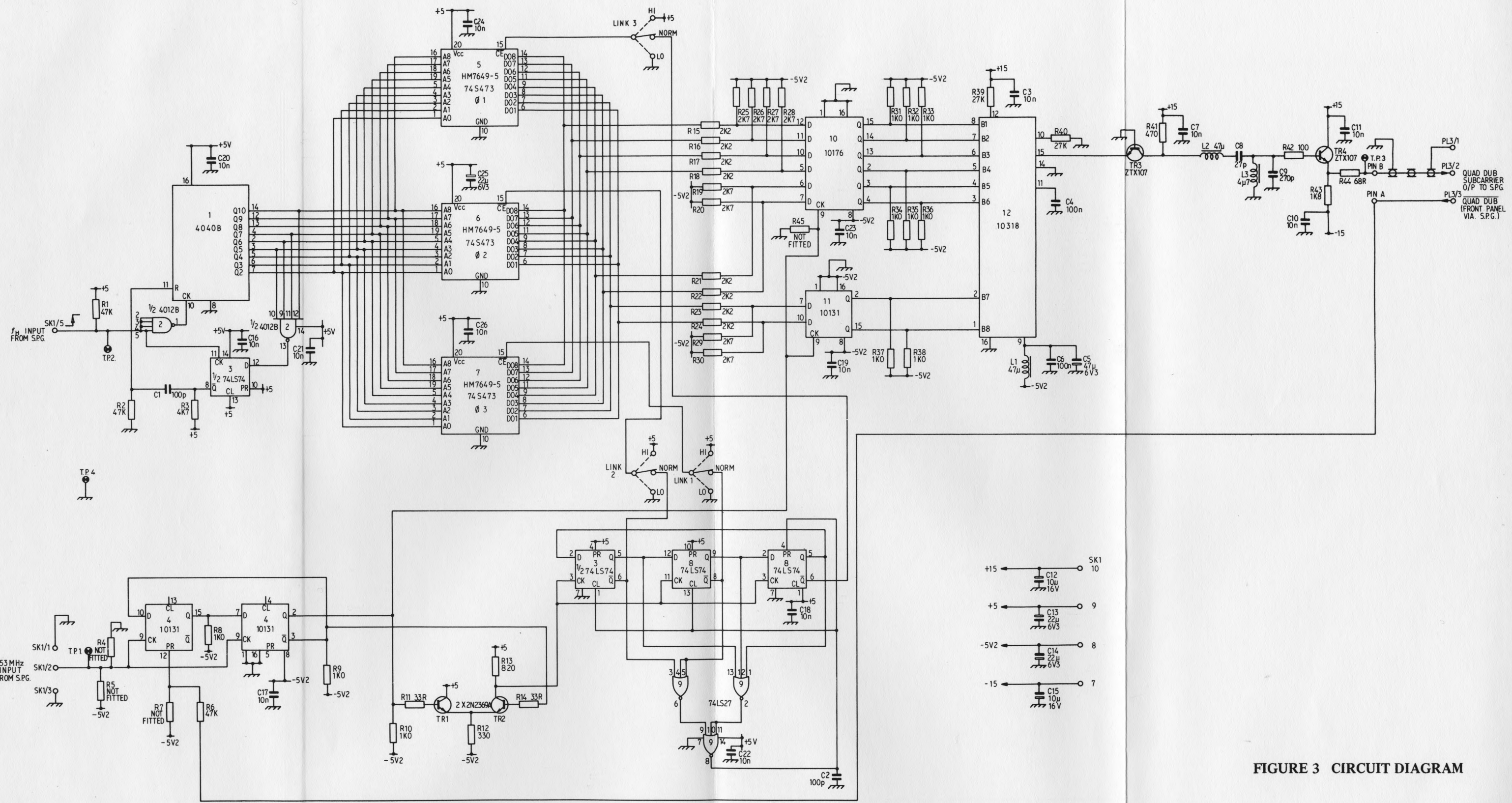


FIGURE 3 CIRCUIT DIAGRAM

POWER

POWER ARRANGEMENTS

INTRODUCTION

1

FIGURE 1 CIRCUIT DIAGRAM, MAINS
INCOMING SUPPLY

FIGURE 2 POWER DISTRIBUTION

POWER ARRANGEMENTS

INTRODUCTION

The 2A mains fuse is mounted on the rear panel adjacent to the POWER IN plug. The incoming supply is switched into the TBC circuits by the POWER ON/OFF switch on the front panel, and applied to the power supply unit via connector B and the Soft Start card. The power supply unit, along with a $\pm 15V$ Regulator card and a $-5.2V$ Regulator card, provide the voltages required by the TBC-2002, and these are distributed to the

printed circuit cards via connector A.

The power supply unit comprises four Farnell G30 power supplies connected in parallel. Note that early PSUs, i.e. those with serial numbers 010 through to 026, comprise four Gould power supplies. If your TBC contains a Gould PSU, please refer to Appendix 1 for additional information.

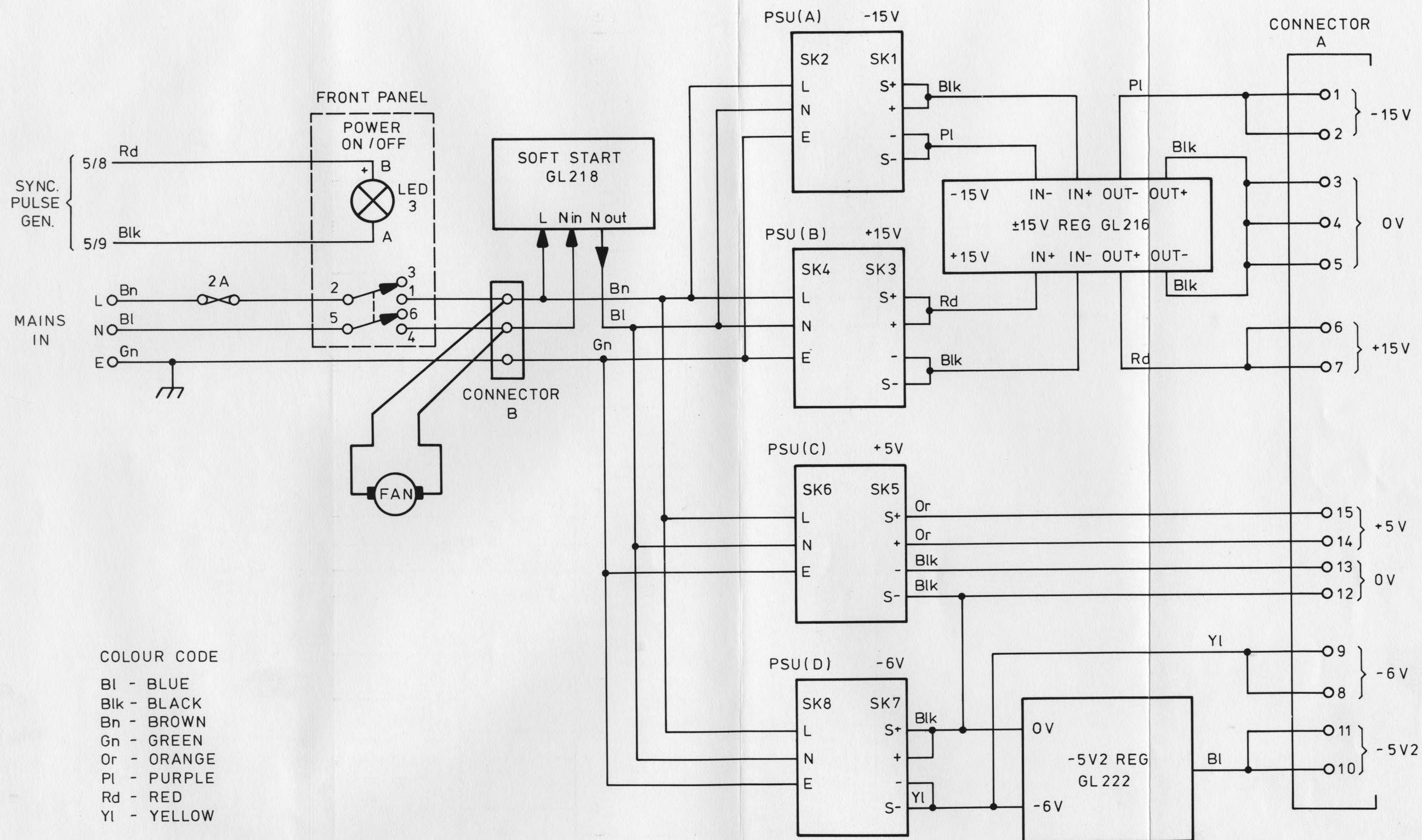


FIGURE 1 CIRCUIT DIAGRAM, MAINS INCOMING SUPPLY

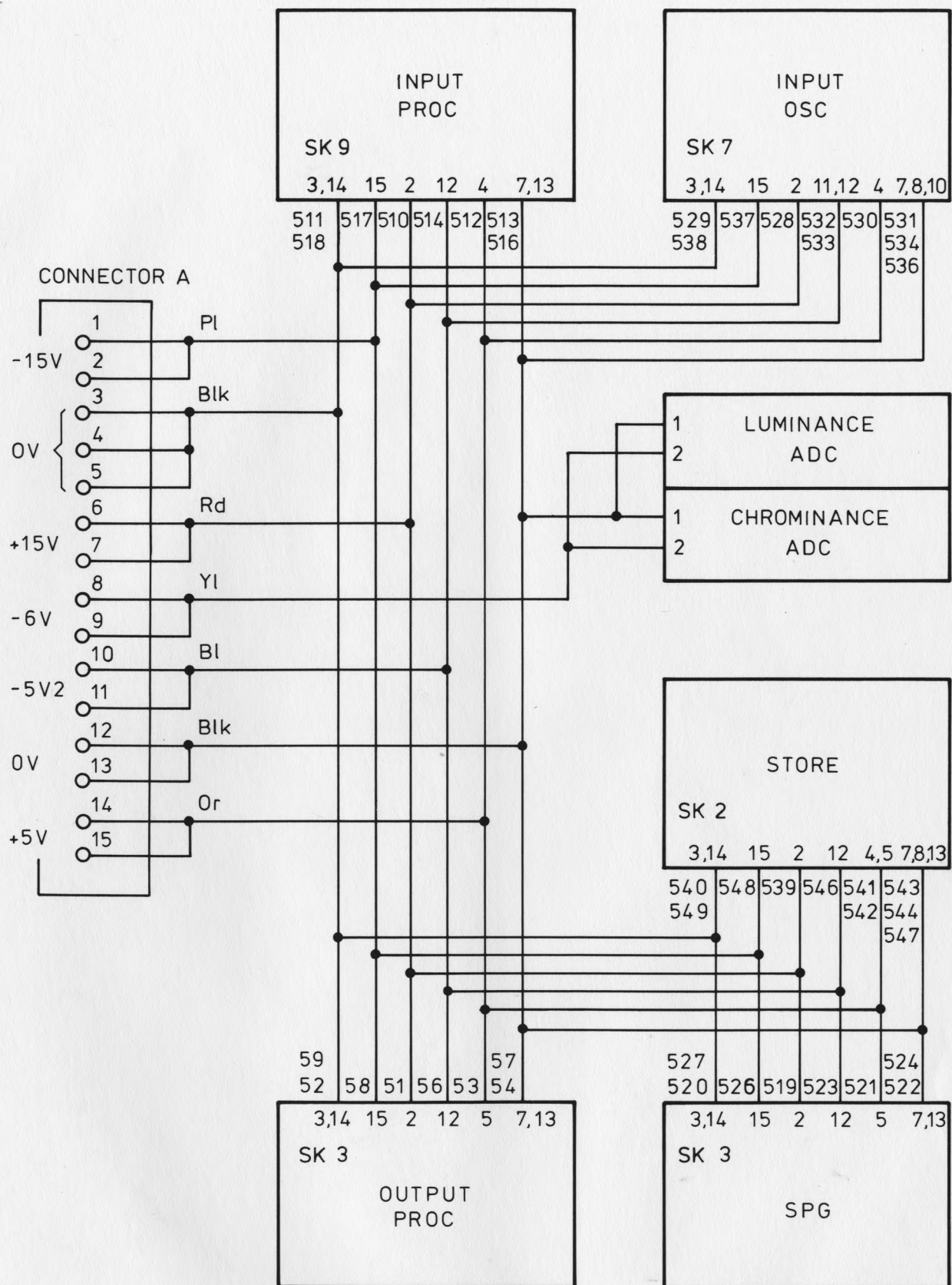


FIGURE 2 POWER DISTRIBUTION

**SOFT START
IVC PCB GL218**

INTRODUCTION	1
CIRCUIT DESCRIPTION	1
ADJUSTMENTS	1
CONNECTIONS	1
COMPONENT SCHEDULE	2

FIGURE 1 COMPONENT LAYOUT

FIGURE 2 CIRCUIT DIAGRAM

SOFT START IVC PCB GL218

INTRODUCTION

The purpose of this card is to limit the current surge on "switch on" into the reservoir capacitors on the switch mode PSU units.

This is carried out by inserting a resistor (R2) in series with the neutral mains input. A TRIAC TR1 is placed across this resistor. When the mains is first applied, there are no firing pulses to TR1 and the surge current is limited by R2. After a few hundred milliseconds, the firing angle of the TRIAC is advanced slowly until it is firing over most of the mains input cycle.

CIRCUIT DESCRIPTION

When the mains voltage is first applied, C5 and C6 are completely discharged. Mains current flows through R1 to charge C1 and C2. The ac current through C1 flows through the bridge rectifier D9 - D12 and charges C5 first, and C6 when the voltage on C5 exceeds 12V. Therefore, initially C1 is effectively in parallel with C2 and the delay due to R1 and the C1, C2 combination is such that the voltage across C2 does not rise sufficiently to fire the 30V DIAC D3.

As C5 and C6 charge up, the diode bridge is progressively back-biased so that the effective value of C1 is reduced. After about a second the bridge is completely back-biased and C1 is effectively out of circuit.

D3 fires many times each half cycle. TR2 is normally biased off, but is turned on to discharge C5 and C6 quickly when the mains supply is interrupted.

ADJUSTMENTS

No adjustments are provided on this card. If, however, it is thought necessary to work on this card, the use of a mains isolating transformer is strongly advocated.

CONNECTIONS

Connections to and from this card are hard-wired to pins as follows:-

L	Brown
Nin	Blue
Nout	Blue

CIRCUIT REF.	DESCRIPTION	PART NO.
	CAPACITORS	
C1	2.2 μ F, 160V	R522257
C2	47nF, 250V	R524738
C3	4700pF, 25V	R504723
C4	1 μ F, 35V	R541054
C5	22 μ F, 35V	R562264
C6	100 μ F, 25V	R561073
C7	220nF, 400V AC	R522248
	DIODES	
D1	1N4148	R354148
D2	1N4148	R354148
D3	DIAC 30V	R390030
D4	35V $\pm$ 5%, 400mW	R399353
D5 – D14	1N4148	R354148
D15	ZF 12V $\pm$ 5%, 400mW	R398012
	RESISTORS	
R1	47k $\pm$ 5%, 2W	R406476
R2	270k, 2.5W	R484274
R3	Not fitted	—
R4	1k0, $\frac{1}{3}$ W	R401105
R5	470k, $\frac{1}{3}$ W	R401477
	TRANSISTORS	
TR1	TRIAC 800V 8A	R340880
TR2	ZTX107L	R348107

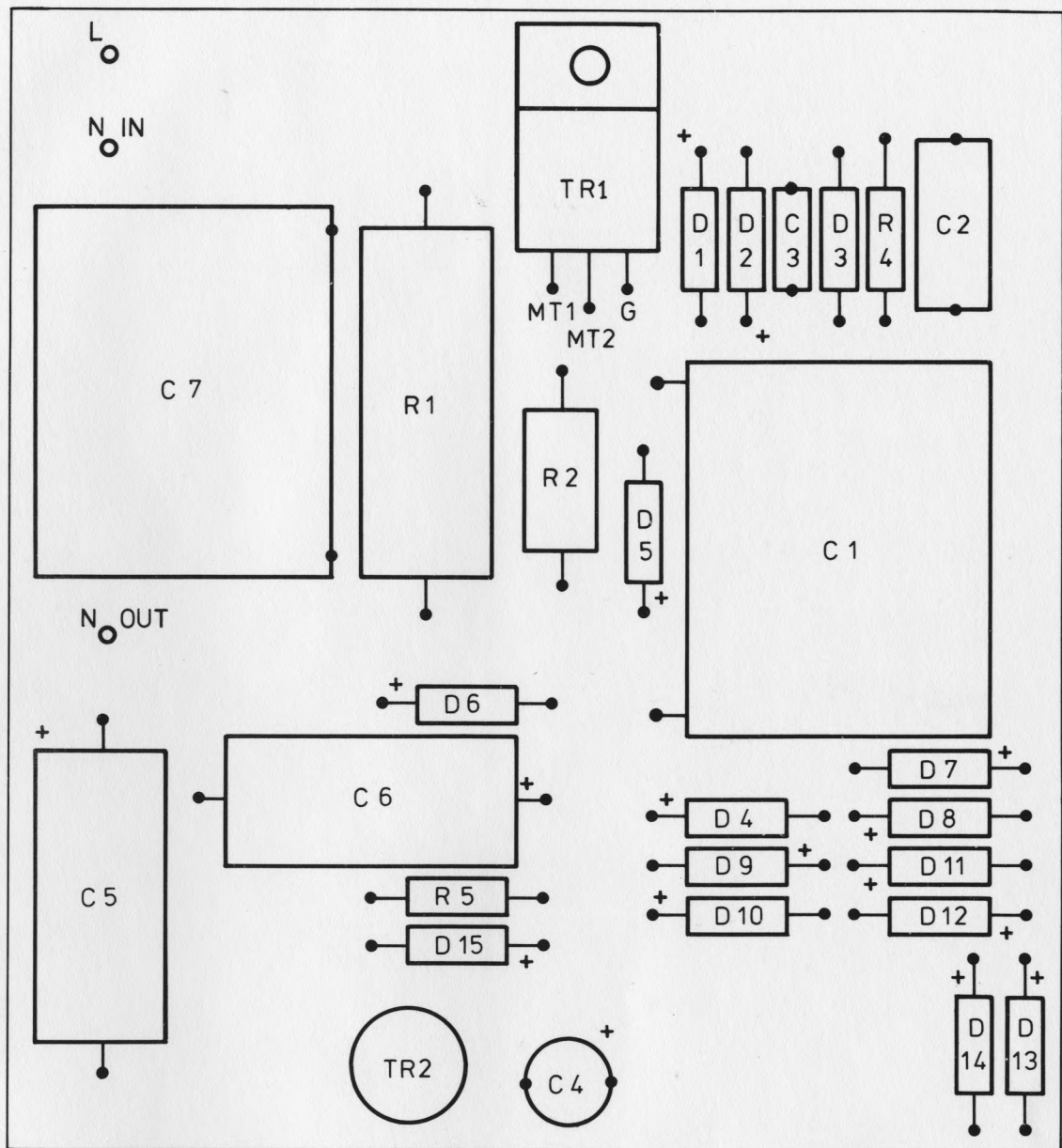


FIGURE 1 COMPONENT LAYOUT

**± 15V REGULATOR
IVC PCB GL216**

DESCRIPTION	1
ADJUSTMENTS	1
CONNECTIONS	1
COMPONENT SCHEDULE	2

FIGURE 1 COMPONENT LAYOUT

FIGURE 2 CIRCUIT DIAGRAM

±15V REGULATOR IVC PCB GL216

DESCRIPTION

The ±15V Regulator card contains two identical circuits which act as filter circuits for the -15V supply from PSU(A) and the +15V supply from PSU(B). The filter circuits remove the low level of switching noise present on the PSU outputs.

Each circuit is a conventional series regulator except that the input voltage also acts as the reference, i.e. the input voltage is divided by R1 and R2 and compared at IC1/3 with the output voltage divided by R4 and R3 at IC1/2. The outputs are distributed to the printed circuit cards in the TBC-2002 via connector A.

ADJUSTMENTS

There are no adjustments provided on this card. If, however, it is thought necessary to work on this card, the use of the mains isolating transformer is strongly recommended.

CONNECTIONS

All connections to and from this card are hard-wired to pins as follows:—

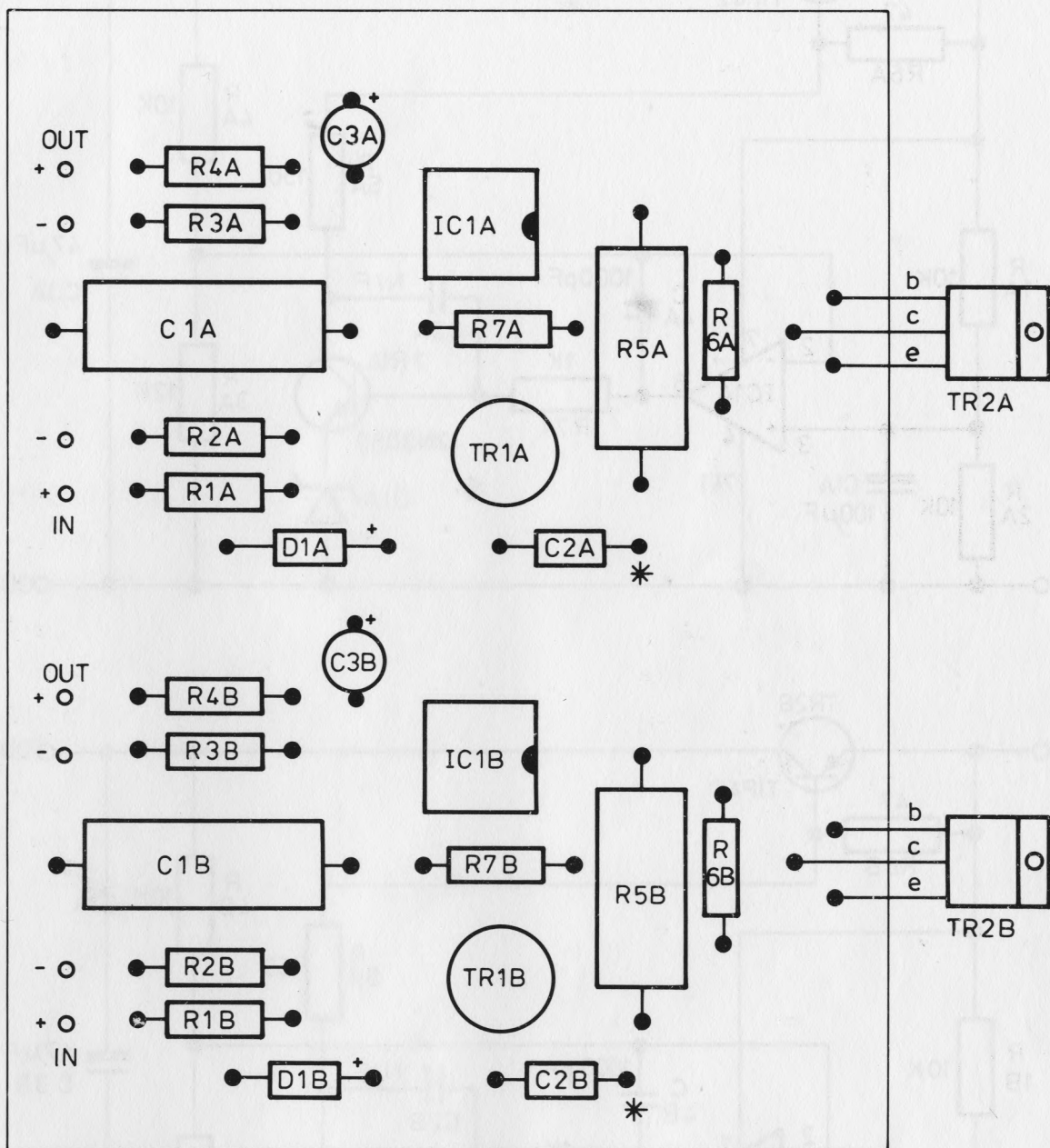
-15V IN+ Black
IN- Purple

OUT+ Black
OUT- Purple

+15V IN+ Red
IN- Black

OUT+ Red
OUT- Black

CIRCUIT REF.	DESCRIPTION	PART NO.
	CAPACITORS	
C1	100 μ F, 10V	R551079
C2	Not fitted	—
C3	47 μ F, 16V	R544762
C4	1,000pF, 63V	R501025
	DIODE	
D1	6.8V Zener	R399682
	INTEGRATED CIRCUIT	
IC1	741	R280741
	RESISTORS	
R1	10k $\pm$ 5%, 0.25W	R405106
R2	10k $\pm$ 5%, 0.25W	R405106
R3	12k $\pm$ 5%, 0.25W	R405126
R4	10k $\pm$ 5%, 0.25W	R405106
R5	150 $\pm$ 10%, 1W	R483154
R6	47R $\pm$ 10%, 0.25W	R405473
R7	1k0 $\pm$ 10%, 0.25W	R405105
	TRANSISTORS	
TR1	2N3053	R303053
TR2	TIP42	R342041



* NOT FITTED

FIGURE 1 COMPONENT LAYOUT

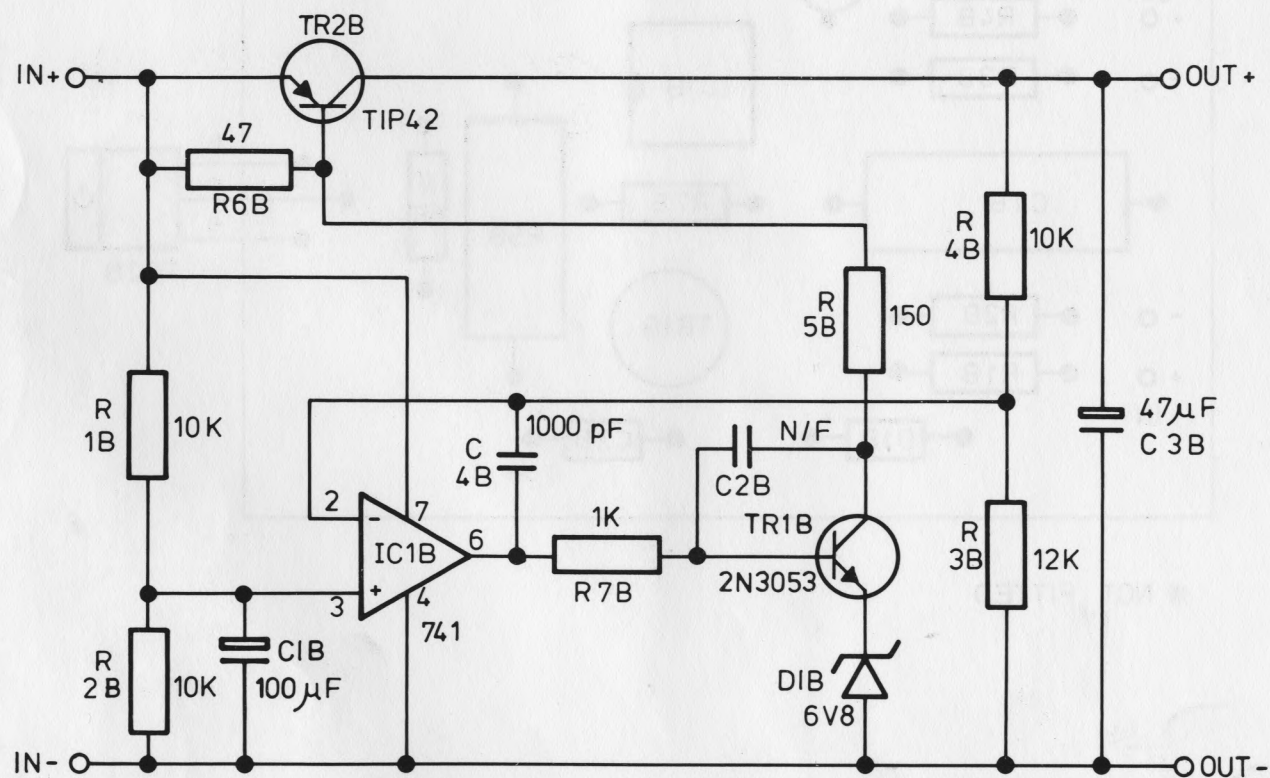
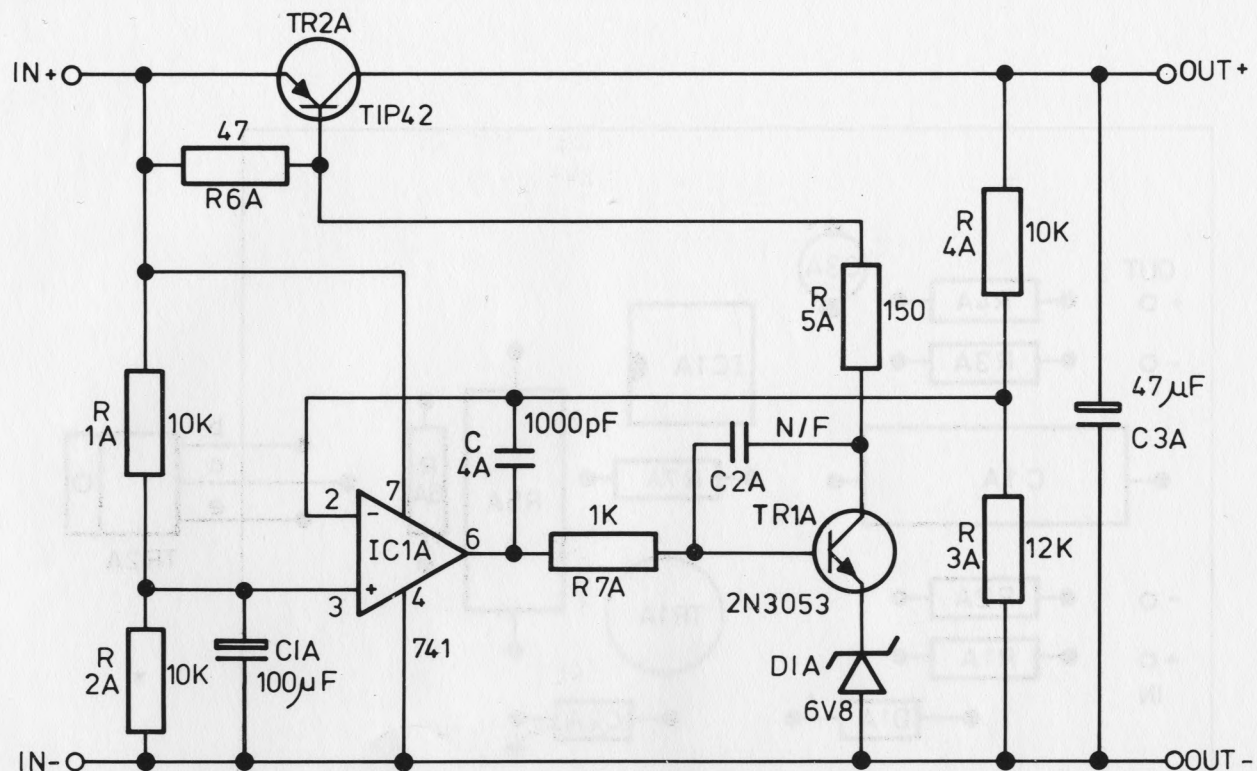


FIGURE 2 CIRCUIT DIAGRAM

**-5.2V REGULATOR
IVC PCB GL222**

DESCRIPTION	1
ADJUSTMENTS	1
CONNECTIONS	1
COMPONENT SCHEDULE	2

FIGURE 1	COMPONENT LAYOUT
FIGURE 2	CIRCUIT DIAGRAM

-5.2V REGULATOR IVC PCB GL222

DESCRIPTION

This card generates the -5.2V supply from the -6V PSU. The -6V supply is used as a voltage reference through R1 and R2 at the base of TR1. The output voltage is divided by R5, R6, R7 to the base of TR2. The -5.2V output is distributed to the printed circuit cards in the TBC-2002 via connector A.

ADJUSTMENTS

No adjustments are provided on this card. If, however, it is thought necessary to work on this card, the use of a mains isolating transformer is strongly recommended.

CONNECTIONS

Connections to and from this card are hard-wired to pins as follows:—

-6V input	Yellow
0V input	Black
-5.2V input	Blue

CIRCUIT REF.	DESCRIPTION	PART NO.
	CAPACITORS	
C1	47 μ F, 16V	R544762
C2	22 μ F, 6.3V	R542261
C3	22 μ F, 6.3V	R542261
	RESISTORS	
R1	1k0 $\pm$ 5%, 0.25W	R405105
R2	1k2 $\pm$ 5%, 0.25W	R405125
R3	560 $\pm$ 5%, 0.25W	R405564
R4	470 $\pm$ 5%, 0.25W	R405474
R5	4k7 $\pm$ 5%, 0.25W	R405475
R6	680 $\pm$ 5%, 0.25W	R405684
R7	1k0 $\pm$ 5%, 0.25W	R405105
	TRANSISTORS	
TR1	ZTX107	R348107
TR2	ZTX107	R348107
TR3	ZTX212	R348212
TR4	TIP41	R342041

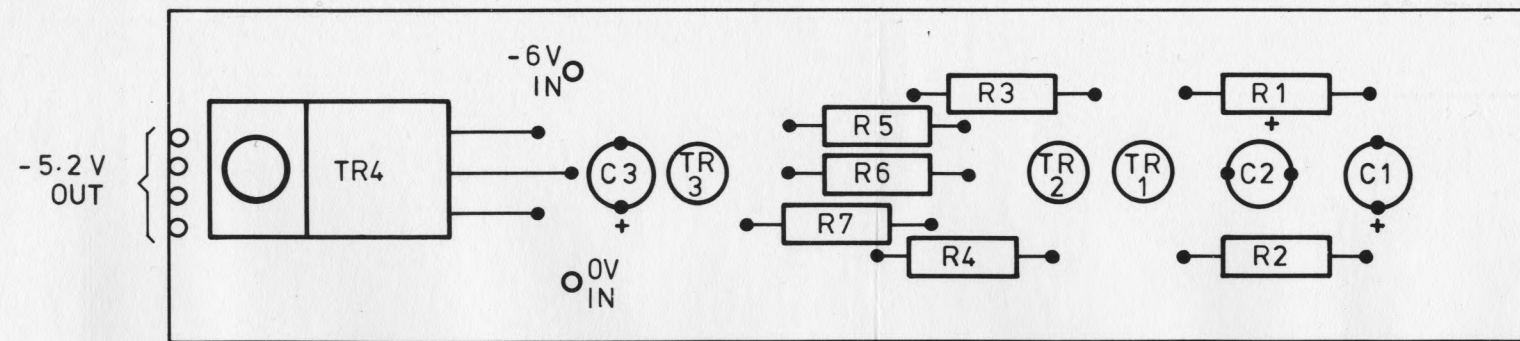


FIGURE 1 COMPONENT LAYOUT

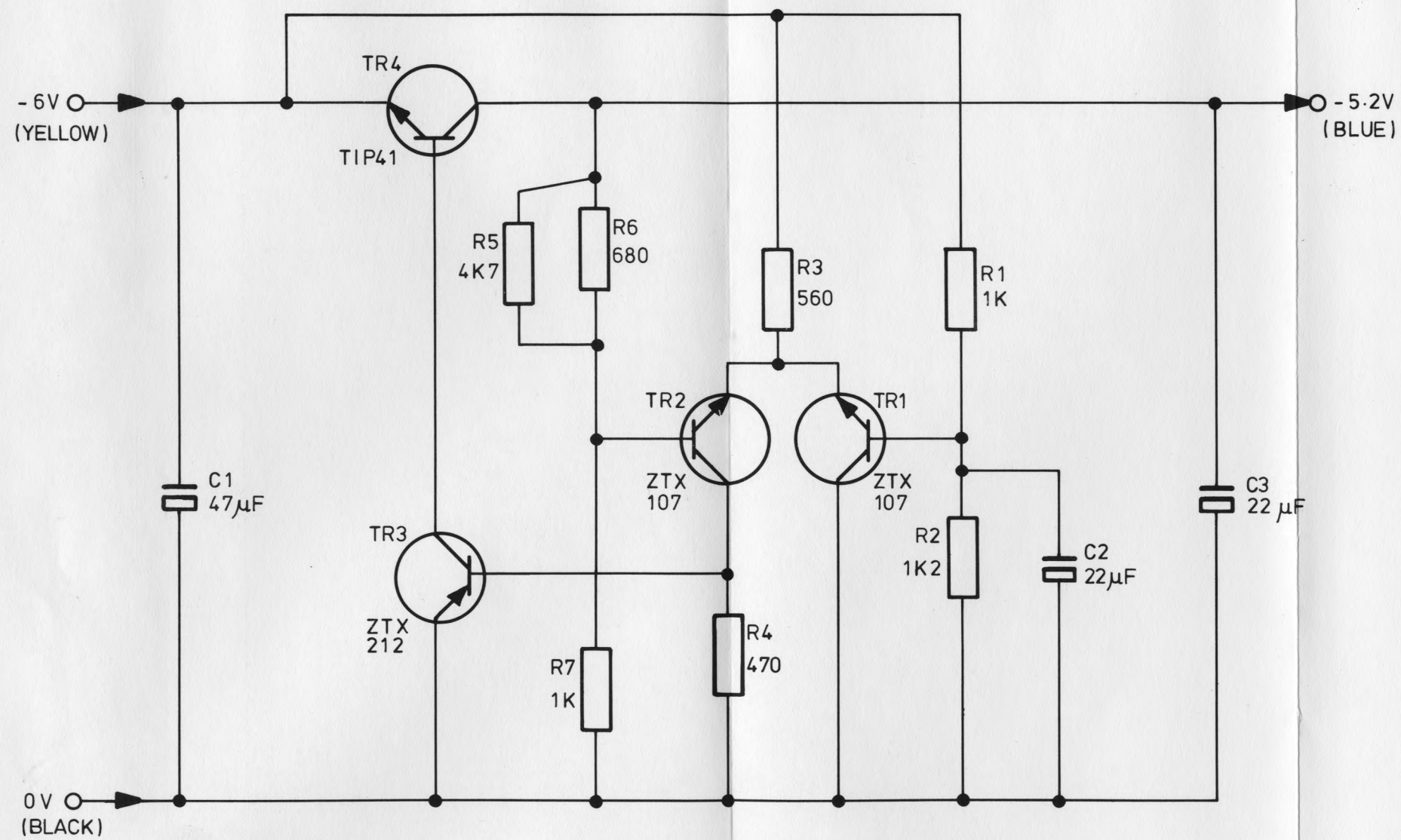


FIGURE 2 CIRCUIT DIAGRAM

**POWER SUPPLY UNIT
FARNELL 30W G RANGE**

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POWER SUPPLY UNIT

FARNELL 30W G RANGE

INTRODUCTION

The Farnell 30 watt G range power supplies use a switching technique to provide stabilised d.c. from a.c. inputs. Use of these techniques has permitted the production of very compact light-weight, high efficiency power supplies which will work from a wide range of mains input voltages.

Four different units are available in the same mechanical package. These are based on combinations of output voltage and current which give a maximum output power of approximately 30 watts.

Each unit will operate from a nominal mains input voltage of either 220 to 240V or 115 to 120V, the range being set by a voltage selector switch on the rear panel.

The output voltage setting may be varied by screwdriver adjustment of the front panel potentiometer and the presence of output voltage is indicated by a front panel L.E.D.

Output current limiting and overvoltage protection are provided. The output voltage may be remotely sensed at the load to correct for voltage drop in the load connecting leads.

The units meet international specifications for conducted radio frequency interference and input to output isolation.

OPERATING INSTRUCTIONS

WARNING!

Hazardous voltages exist at many points within the unit. DISCONNECT THE MAINS INPUT SUPPLY BEFORE OPENING THE UNIT. If the unit requires servicing it is recommended that it be returned to the manufacturer.

MAINS INPUT

The mains input terminals are on the 3 way front

panel terminal block and are marked L (live), N (neutral) and  (earth). The unit will operate from either a 115 to 120V supply or a 220 to 240V supply and this should be set by the voltage selector switch on the rear panel of the unit before connecting the mains input supply. For 115 to 120V operation set the voltage selector to 115V. For 220 to 240V operation set the voltage selector to 230V.

WARNING: INCORRECT SETTING OF THE INPUT VOLTAGE SELECTOR SWITCH MAY RESULT IN DAMAGE TO THE UNIT.

OUTPUT CONNECTIONS

The output connections are taken from the terminals marked '+' and '-' on the 4 way front panel terminal block. Ensure that the '+' terminal is linked to the '+' terminal and the '-' terminal linked to the '-' terminal unless remote sensing is being used. The presence of output voltage is indicated by the front panel L.E.D. adjacent to the terminal block.

CIRCUIT DESCRIPTION

POWER CIRCUITS

The mains input supply is connected through the input filter and bridge rectifier MR101 to reservoir capacitors C105, C106 (for 115V operation MR101, C105 and C106 are connected as a voltage doubler circuit). The resulting d.c. rail of about 340V supplies power via current transformer TX101 to a single transistor forward converter, formed by transformer TX102 and switch transistor VT106. The transformer secondary voltage is rectified by D4 and D5 and then filtered by L1, L2, C9, C14, C15 to produce a d.c. voltage at the output terminals. This d.c. voltage is proportional to the average d.c. level of the pulse waveform on the transformer secondary.

VOLTAGE CONTROL CIRCUIT

A proportion of the output voltage is compared with the reference voltage at Z3 by the voltage control amplifier IC4. Any difference between these two voltages is amplified to produce a d.c. control signal which is coupled by opto isolator IC3 to VT105. This transistor compares the control signal with a voltage ramp developed across C111.

When the ramp voltage exceeds the control signal then VT105 triggers SCR101 which pulls off switch transistor VT106.

Conduction of VT106 is initiated by clock pulses generated at a frequency of 30kHz by PUT101 and VT102. VT106 is maintained in conduction by regenerative feedback from current transformer TX101, until SCR101 conducts. At this point VT106 ceases to conduct until driven by the next clock pulse.

In this way, the conduction time of VT106, and hence the average secondary voltage from transformer TX102, can be varied by the d.c. control signal to stabilise the power supply output voltage.

An overwind on transformer TX102 is used to generate the voltage ramp by charging C111 through R118, when VT106 conducts. Capacitor C111 is discharged when VT106 turns off and the voltage across TX102 drops. An auxiliary supply rail is also derived from the overwind on TX102 to

power VT105 and the current limit amplifier. VT104 and Z101 act as an inhibit on this supply rail to prevent VT106 switching when the mains input is low.

CURRENT LIMIT CIRCUIT

The peak current in transformer TX101, proportional to the power supply output current, is sensed across R119 by the current limit amplifier IC1. This compares the sense voltage with the reference voltage at Z1. If the peak voltage across R119 exceeds a pre-set level then the output of the current limit amplifier falls and overrides the d.c. control signal from the voltage amplifier. The conduction time of switch transistor VT106 is reduced and the output voltage of the unit falls sufficiently to limit the output current to a safe value.

OVERVOLTAGE PROTECTION CIRCUIT

A proportion of the unit output voltage is compared with the voltage across Z2 by the overvoltage amplifier VT1, VT2. If the output voltage exceeds a pre-set level then the overvoltage amplifier provides a drive signal which is coupled through opto-isolator IC2 to a transistor latch formed by VT101, VT103. When this latch is triggered the clock is inhibited and VT106 ceases to switch, giving complete shut-down of the power supply. The latch stays in the triggered condition until the mains input supply is interrupted for a few seconds.

SPECIFICATION

MAINS INPUT	220 to 240V or 115 to 120V set by voltage selector switch 45 to 440MHz.			
MAINS VARIATION TOLERATED	220V-20% to 240V + 10%. 115V-20% to 120V + 10%.			
OUTPUTS	Unit	Nominal output voltage	Max. output current	Voltage adjust range
	G6-5M	6V	5A	4 to 6V
	G15-2M	15V	2A	10 to 16.5V
OUTPUT VOLTAGE REGULATION	0.1% maximum variation for a worst case of combination of 0 to 100% load change and 220V - 10% to 240V + 10% or 115V - 10% to 120V + 10% line change.			
RIPPLE AND NOISE at full load (30MHz bandwidth)	Less than 10mV r.m.s.; 50mV pk to pk.			
TEMPERATURE COEFFICIENT	± 0.01% per °C typical.			
TRANSIENT RECOVERY TIME	Typically 1mS for output to recover within 50mV following a 10% to 100% to 10% load change of 5µS risetime..Typical instantaneous output deviation 400mV.			
OPERATING AMBIENT TEMPERATURE RANGE	-10°C to +55°C for full load output current. Convection cooled free air rating.			
MAXIMUM OPERATING AMBIENT TEMPERATURE	70°C max. Output current should be derated linearly from full load at 55°C to half load at 70°C.			
STORAGE TEMP. RANGE	-40°C to + 85°C			
HOLD-UP TIME	Output will be maintained for the duration of a missing mains cycle (28mS) at maximum output current and 220V - 10% or 115V - 10% mains input, when the output is at 6V for 6V nominal units or nominal +5% for other units			
SWITCH ON SURGE	Less than 80A			
SWITCH ON TIME	Output established within 30mS			
INSULATION	Tested at 2.1kV peak for 1 minute between a.c. input and d.c. output, with output terminals and earth connected together. ± 250V d.c. continuous rating between output and earth. Tested to 500V d.c. for 1 minute.			
REMOTE SENSING	Up to 5V max. drop in each output lead permitted. However unit output terminal voltage must not exceed 6V for nominal 6V units, or nominal +5% for other units.			

SPECIFICATION (continued)

EFFICIENCY

Better than 70% at full load.

PROTECTION

Overload

Constant current limiting set at $110\% \pm 5\%$ of full load current

Overvoltage

Set at nominal output voltage $+20\%$. Disables control circuit and output falls to zero. Reset by interrupting the mains input supply.

Fuse

The a.c. input is fused (fuse type 1A.T.)

RADIO FREQUENCY INTERFERENCE

Units will comply with the conducted interference requirements of VDE0875 curve N, CISPR (publication 2) curve N and BS800

DIMENSIONS (excluding terminals)

145 x 88 x 33mm

WEIGHT

750g

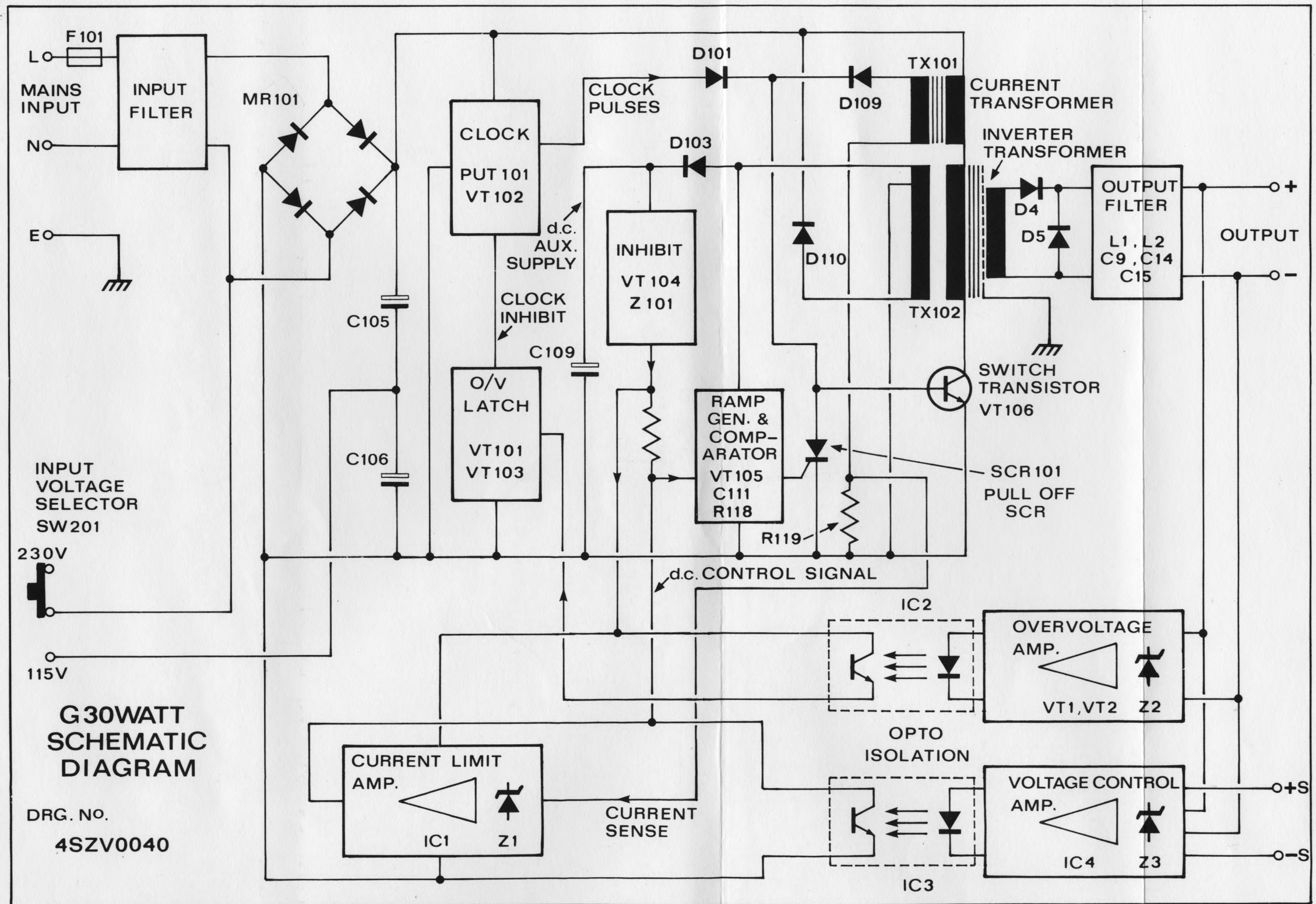
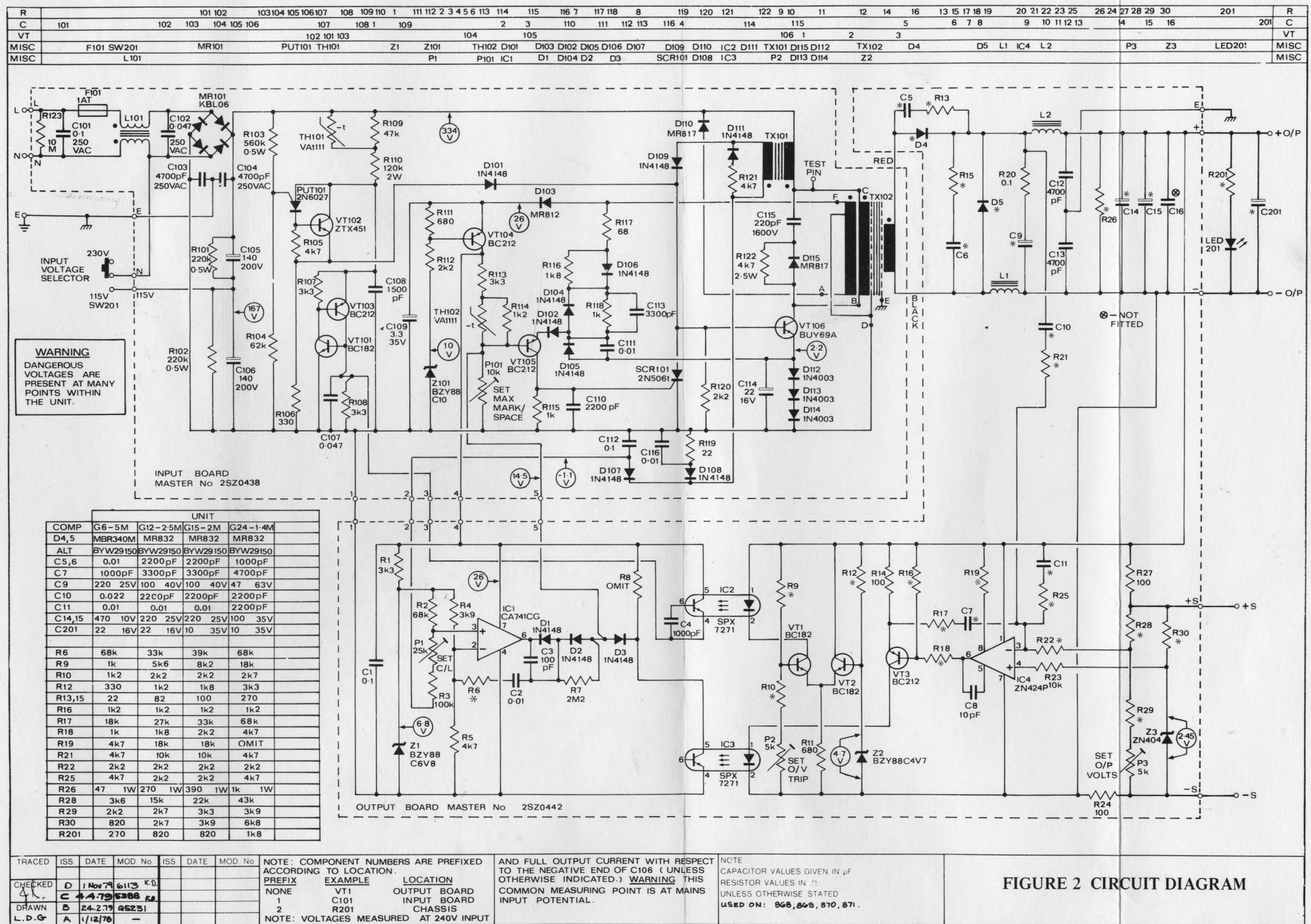


FIGURE 1 BLOCK DIAGRAM



APPENDIX 1

GOULD POWER SUPPLY UNITS

Power supply units with serial numbers 010 through to 026 comprise two type MMG5-5 and two type MMG15-2 Gould power supplies.

Although the power arrangements are similar to those for the Farnell units, please note the following:—

- a) Connections to and from the PSU are via one barrier connector as shown below.
- b) The Soft Start card GL218 and $\pm 15V$

Regulator card GL216 are included and are mounted inside the PSU cover.

- c) The $-5.2V$ Regulator card GL222 is included only for those PSUs with the serial numbers listed below, and it is mounted on the Output Filter card GL209.

019, 020, 021
024, 025, 026

